Hot Carrier Reliability of N-LDMOS Transistor Arrays for Power BiCMOS Applications

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ABSTRACT

This paper evaluates the hot carrier performance of n-channel lateral DMOS (N-LDMOS) transistors. The N-LDMOS has been the common choice for the driver transistor in high voltage (20-30 V) smart power applications. These high drain voltages potentially make N-LDMOS hot carrier degradation an important reliability concern. This paper focuses on the hot carrier test methodology and geometry effects in N-LDMOS transistor arrays. This paper differs from previous work in that it describes for the first time the HC performance of N-LDMOS transistor arrays rather than discrete devices and discusses an N-LDMOS failure mode not yet addressed in the literature.

INTRODUCTION

Smart power management devices require IC devices in the 20-30 V range. These circuits often combine high performance CMOS and bipolar transistors with a power MOS driver. Applications include voltage converters, mobile phones and internet appliances. The N-LDMOS is a common choice as the driver transistor [1,2]. Due to the high drain voltages used in these applications LDMOS hot carrier (HC) degradation is an important reliability concern [3]. In power management applications the LDMOS device often operates as a switch with two static bias states On and Off. In the On state the drain to source voltage (Vds) is a few tenths of a volt and gate to source voltage (Vgs) is near 5 volts. In the Off state the Vds is > 20 V and the Vgs is near 0 volts. Neither On nor Off bias points are expected to yield significant LDMOS HC degradation instead HC effects are expected to occur during transients when both Vgs and Vds are simultaneously high [4,5].

The N-LDMOS cross section considered in this study is shown in Figure 1. This device features an extended drain region under the field oxide (FOX) consisting of an n-drift region and an n-layer for on-resistance (Rdson) control. The polysilicon gate (Poly Gate) overlaps the gate oxide and extends over the field oxide. Device area is minimized by connecting the source and p-body to a common terminal. The device threshold voltage (Vt) is ~ 1.0 V. Important LDMOS performance parameters are low Rdson and high drain breakdown voltage. A critical LDMOS layout parameter is the length L between the field oxide drain and source edge since this distance must sustain the high LDMOS drain voltages.

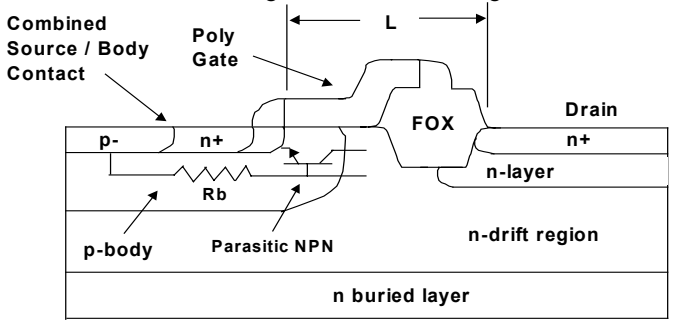

Figure 1. Schematic cross section of N-LDMOS device.

To obtain high drive currents and minimal Rdson, LDMOS devices are often implemented in a checkerboard array of transistors. Figure 2 depicts a schematic view of an 8 source LDMOS array. Transistor arrays are composed of unit cells consisting of a single source and drain. Metal routing ties all sources (and drains) together creating a parallel device structure. A separate connection to the polysilicon gate controls the resistance of the device. Advantages of transistor arrays include high current capability with minimum power dissipation and more uniform current flow per device area.

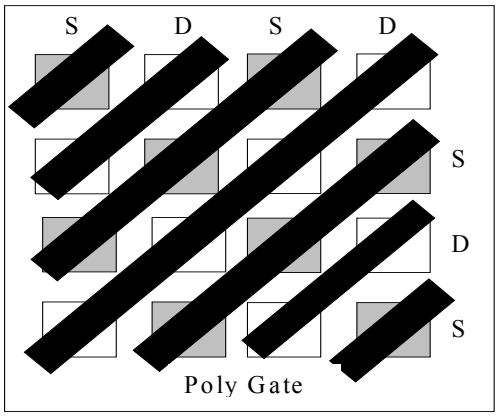

Figure 2. Schematic view of an 8 source LDMOS array. In LDMOS arrays all sources (S) are connected together and drains (D) are connected together to form a parallel device structure.

LDMOS HC stress conditions can not be arbitrarily chosen. At high Vds and Vgs LDMOS devices exhibit a destructive snapback region [6] due to the intrinsic parasitic NPN bipolar transistor shown in Figure 1. This snapback region limits the LDMOS operating envelope and HC stress bias conditions to an electrical safe operating area (SOA) as seen in Figure 3. In this particular case, though, HC stress conditions are defined by circuit design requirements of 120 μA per source and a maximum operating (use) voltage of 24 V. This corresponds to a Vgs that is ~0.5 V above the transistor threshold (Vgs ~ 1.5 V). Figure 3 shows that this operating point is well within the SOA of the device.

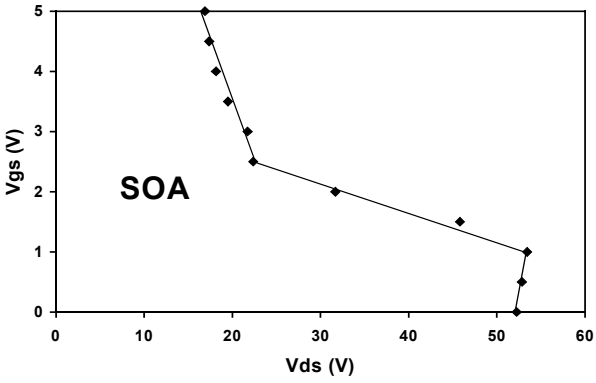

Figure 3. N-LDMOS safe operating area (SOA).

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EXPERIMENTAL DETAILS

The devices used in this study are discrete (single source and drain), 50 source and 200 source N-LDMOS arrays. All devices were tested at wafer level using a Keithley S400 parametric test system. Because N-LDMOS arrays have low on-resistance (~5 Ω for 200 source array), two pads are connected to each array source and drain. These additional pads allow Kelvin monitoring and compensation of applied voltages during both stress and parametric measurements minimizing the effect of probe series contact resistance on measurement results.

A test issue arises when applying the constant drain current (120 μA per source) during stress. This current corresponds to a gate stress voltage that is ~0.5V above the device threshold voltage. This is an issue because normal threshold voltage variations can cause large variations in the actual drain stress current. A search technique could potentially be used to obtain the proper Vgs, but drain current overshoot during search could cause erroneous HC device degradation. Instead, a floating source stress technique is used as shown in Figure 4. In this technique SMU2 sinks the source current (Istr) ensuring a constant drain to source stress current while the floating bias supply SMU1 applies the required drain to source stress voltage (Vdstr).

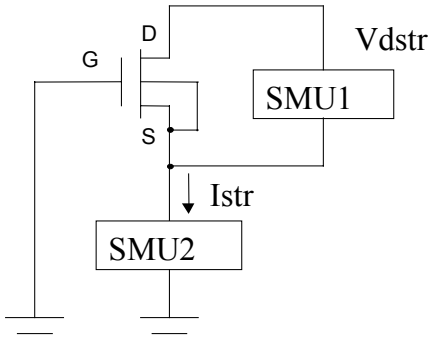


Figure 4. Floating source stress technique.

During hot-carrier testing device parameters are monitored before and after device stress. Stress times are typically logarithmic time intervals (e.g. 10s, 30s, 100s, 300s, etc.). Monitored device parameters include the saturation drain current (Idsat) determined at Vgs ~1.5 V and Vds = 24V, Rdson at Vgs = 5V, Vds = 0.1 V, Vtext (extrapolated threshold voltage) and GMmax (maximum slope transconductance) at Vds = 0.1 V.

EXPERIMENTAL RESULTS

Hot carrier degradation results

Figure 5 displays typical HC degradation results from a 50 source N-LDMOS array for parameters Idsat, Rdson, Vtext and GMmax. This data was obtained from the initial device layout design biased at the use bias conditions (120 μA per source and Vds = 24 V). Figure 5 shows that the parameter Rdson has the greatest rate of degradation and increases with time. The parameter GMmax decreases with time and displays the second greatest degradation rate. Figure 5 also shows that the degradation slope of GMmax and Rdson are approximately equal, indicating similar degradation mechanisms for the two measurement parameters. It is also seen in Figure 5 that Idsat and Vtext degradation is minimal.

For power switching devices the series on-resistance Rdson rather than Idsat is the critical electrical parameter and 10% degradation in Rdson is defined as the N-LDMOS device lifetime. Figure 5 shows that N-LDMOS Rdson HC degradation can be substantial even at use bias conditions with the 10% degradation point occurring in <50k sec (13.9 hrs). This result falls well short of meeting the 10 year HC target lifetime requirement for this array.

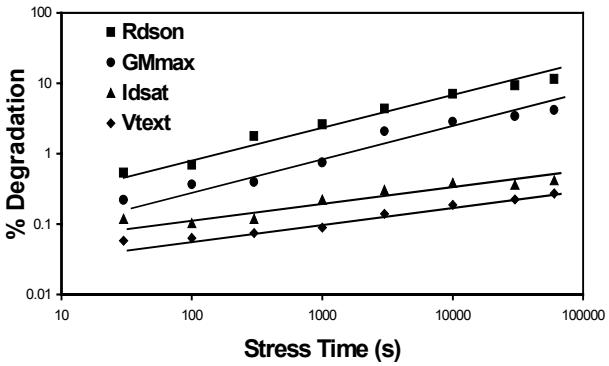
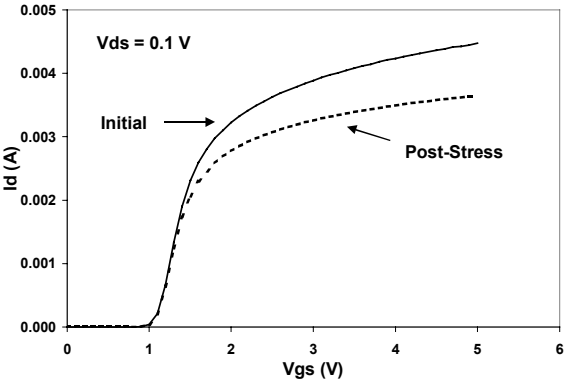


Figure 5. Typical N-LDMOS (50 source array) HC degradation for parameters Rdson, GMmax, Idsat and Vtext.

Figure 6 displays the effects of 30k seconds Vds = 32 V HC stress on N-LDMOS (50 source array) drain current (Id) output characteristic. Figure 6 shows that while the stress causes substantial degradation (~20%) at Rdson bias conditions (Vds =0.1 V, Vgs = 5.0 V), minimal changes (~0.5%) occur at the saturated (Idsat) bias conditions (Vgs =1.5 V and Vds = 24 V). These results are in qualitative agreement with the parameter degradation results shown in Figure 5.



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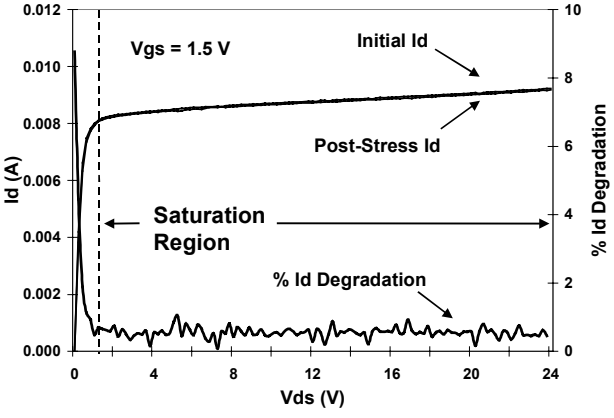


(b)

Figure 6. Effect of a 30k second 32 V HC stress on N-LDMOS (a) linear and (b) saturation drain current (Id) output characteristics.

N-LDMOS hot carrier degradation mechanism

Figures 5 and 6 show that Rdson degrades much more rapidly than Idsat. To understand this, 2-D device simulations were performed to determine the current path and impact ionization rate at the Rdson and Idsat bias points. These plots are shown in Figure 7 and 8. Adjacent current lines in Figure 7 represent 5% of the device current. Comparing Figure 7 and 8, it is seen that at the Rdson bias conditions, the current path is along the Si-SiO_2 interface. This differs from the Idsat bias conditions where the current path is well below the Si-SiO_2 interface. Therefore, Si-SiO_2 HC generated interface damage should have maximum impact on Rdson and minimal impact on Idsat. These simulation results are in qualitative agreement with the degradation results shown in Figure 5. Figure 8 also shows that at use bias conditions, the maximum impact ionization point is within the extended drain region of the N-LDMOS device near the Si-FOX interface. This differs from conventional NMOS devices where the maximum impact ionization occurs in the device channel near the drain under the gate oxide.

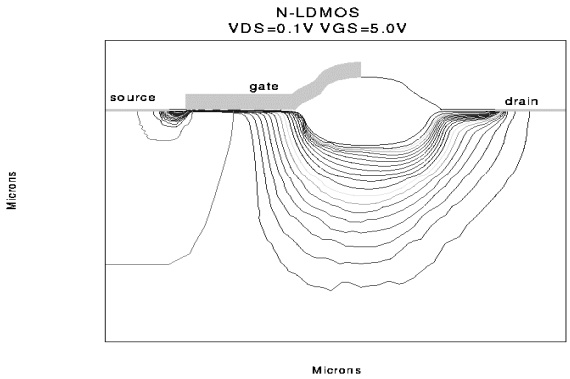


Figure 7. Simulated drain to source current flow at Rdson bias conditions.

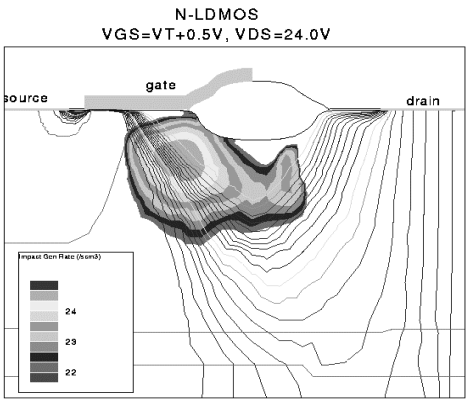
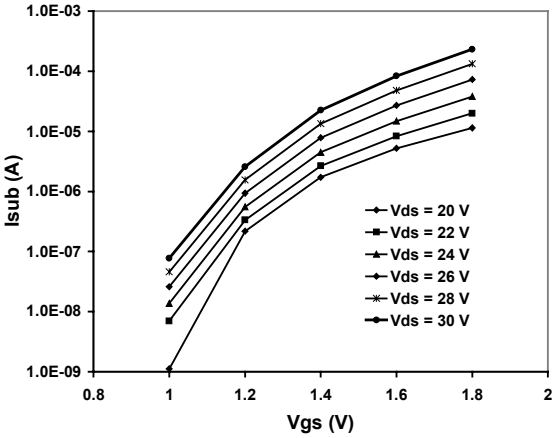


Figure 8. Simulated drain to source current flow and impact ionization rate contours (shaded areas) at Idsat (use) bias conditions.

In conventional NMOS, electrons are accelerated to high velocities by the large lateral electric fields in the pinch-off region near the drain of the device. These high velocity electrons cause impact ionization creating electron-hole pairs. Excess holes result in increased substrate current. A small percentage of these carriers may attain enough energy to be injected into the gate oxide resulting in a measurable gate current. Measuring the N-LDMOS gate and substrate current should provide important information concerning the N-LDMOS degradation mechanism. Figures 9 display N-LDMOS array substrate (Isub) and gate (Ig) current versus Vgs and Vds.



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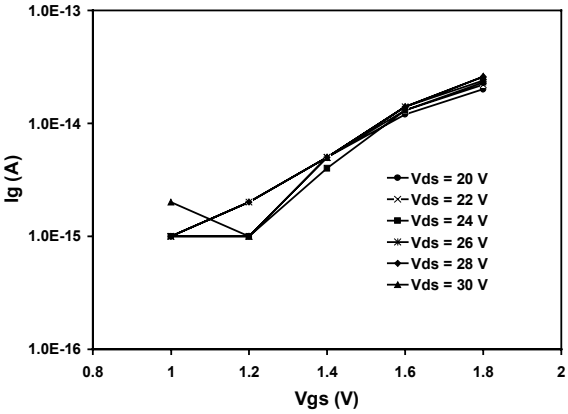


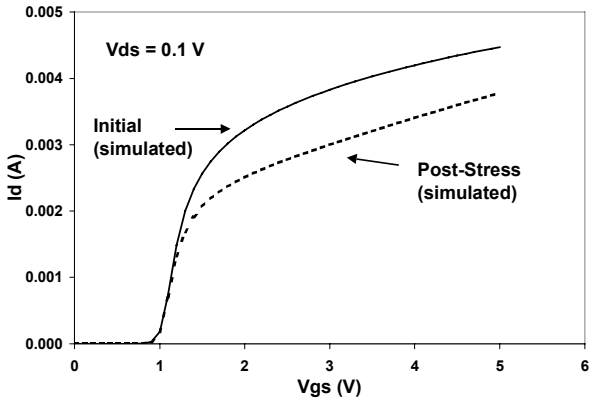
(b)

Figure 9. N-LDMOS (50 source array) Isub (a) and Ig (b) vs. Vgs.

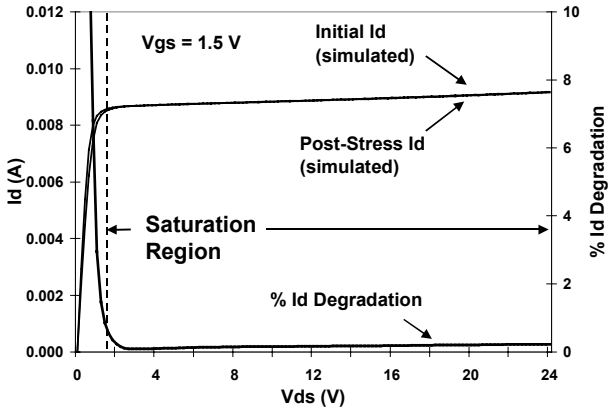
Figure 9 shows that, while the N-LDMOS substrate current is a strong function of drain voltage, no increase is seen in the measured gate current. Figure 9 results coupled with the small Vt shifts seen in Figure 5 indicate that HC injection (hole or electron) into the gate oxide does not play an important role in the N-LDMOS degradation mechanism. Instead, the most probable cause is damage to the Si-FOX interface.

The proposed N-LDMOS degradation mechanism is HC generated interface states (traps) which result in a build up of negative charge at the Si-FOX interface. The location of this negative charge is in the vicinity of the maximum impact ionization point shown in Figure 8. This negative charge attracts holes depleting the negative charge in the LDMOS n-drift region increasing the Rdson device resistance. This effect has the greatest impact on Rdson since the Rdson current path is along the Si-FOX interface.

Figure 10 displays simulated degradation effects in N-LDMOS linear and saturation drain current output characteristics. These simulations were obtained by placing a linearly distributed negative charge ($3x10^{11}/cm^2$) at the Si-FOX interface in the region where the impact ionization contours in Figure 8 intersect the FOX interface. Figure 10 shows the simulated trapped negative charge causes substantial degradation in the linear device behavior but only minimal degradation in device saturation. These results are in qualitative agreement with the N-LDMOS measured HC parameter degradation results shown in Figure 5 and the output HC degradation curves shown in Figure 6.



(a)



(b)

Figure 10. Simulated effect of placing a linearly distributed negative charge at the Si-FOX interface on the N-LDMOS linear (a) and saturation (b) output characteristics.

N-LDMOS discrete versus array results

Table 1 displays relative Rdson lifetime results from both N-LDMOS discrete and arrays stressed at target use condition (120 μA per source and Vds =24 V). In these measurements, the discrete device consists of a single source and drain and has identical layout spacing and source-drain dimensions as the 50 source and 200 source array. Table 1 shows that discrete device HC results differ greatly from arrays and significantly overestimates the HC performance.

Table 1. Discrete (1 source) vs. array Rdson lifetime results

Device	Relative Rdson Lifetime
Discrete	37.09
50 Source Array	1.12
200 Source Array	1.00

The reason for this is evident in the discrete device top view simulation shown in Figure 11. Figure 11 displays simulated drain to source current flow and electric field (E) contour lines (shaded areas). Figure 11 shows that for discrete devices only about 50% of the stress current travels through the maximum electric field contour of device (labeled Emax in Figure 11). This differs from arrays where the majority of the current is expected to pass through the maximum electric field contour. Figure 11 shows that, for discrete devices, the stress current density is effectively reduced improving the hot carrier performance of discrete devices relative to arrays. It is clear from Table 1 and Figure 11 that discrete device HC performance does not scale to arrays. This study, therefore, focuses on the HC performance N-LDMOS arrays.

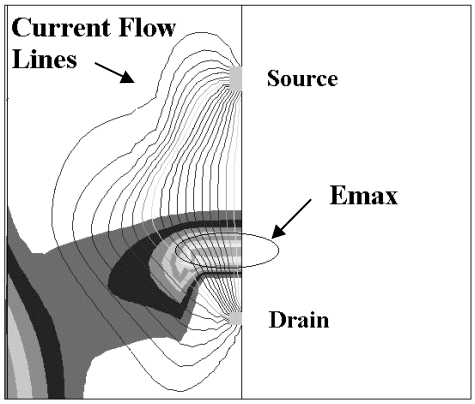


Figure 11. Simulated current flow lines and electric field contours (shaded areas) of a discrete N-LDMOS device at stress bias conditions.

Hot Carrier lifetime results and models

Since N-LDMOS lifetimes are expected to be long (>10 years), accelerated stress techniques must be implemented to determine the HC lifetime. The accelerated stress methodology relies on degradation and lifetime models to predict device lifetime. It is not evident that traditional NMOS models can be applied to the N-LDMOS devices. Potential issues that exist include differences between the NMOS and N-LDMOS HC degradation mechanisms and the additional complication of using N-LDMOS arrays as the test vehicle. Because of these issues, it is necessary to validate degradation and lifetime models for the N-LDMOS array.

Conventional NMOS parameter degradation (Y) as a function of time (t) is typically described by a power law:

$$Y(t) = Ct^n \tag{1}$$

where C is a constant and n the degradation exponent. In conventional NMOS a degradation exponent n of 0.5-0.7 is typical of interface trap generation [7]. This model is verified by plotting the log of the degradation versus the log of stress time and should be linear if the data exhibits power law behavior. For NMOS lifetime prediction, the substrate current lifetime model [8] is often used and is given by:

$$Tau * Id = C\left(\frac{Isub}{Id}\right)^{-m} \tag{2}$$

where Tau is the device lifetime, Id the drain current and Isub the device substrate current. The parameters C and m in Equation 2 are the lifetime acceleration factor and exponent, respectively. In conventional NMOS, the lifetime exponent m is a function of the amount of energy required to create an interface trap divided by the impact ionization energy and typically has a value ~3.

It is evident from Figure 5 that N-LDMOS array degradation data demonstrates power law behavior (Equation 1) and that this power law behavior extends over wide range of time magnitudes. In

Figure 5, the Rdson and GMmax degradation exponent n were 0.420 and 0.416, respectively. This power law degradation behavior was observed for all tested N-LDMOS device layouts (discrete devices and arrays) with the exponent n ranging from 0.36-0.65. Figure 12 displays N-LDMOS array Rdson lifetime versus substrate current. This data was obtained from a specially designed N-LDMOS device with separate substrate and source contacts. Figure 12 clearly shows that Rdson degradation is described by Equation 2 (fit correlation coefficient R^2=0.997) with a lifetime exponent m of 2.34.

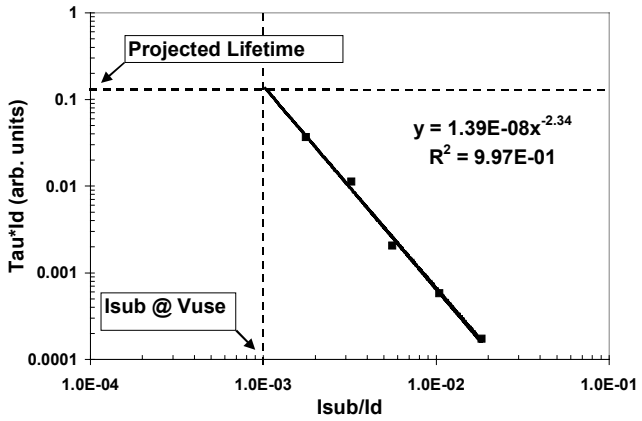


Figure 12. N-LDMOS (50 source array) Rdson lifetime (Tau) vs. substrate current (Isub).

In practical N-LDMOS arrays the source and p-body are shorted together at the chip level to minimize device area, thus substrate current cannot be measured and Equation 2 can not be applied to lifetime prediction. Figure 13 shows that Rdson degradation lifetime data can also be fit (R^2=0.993) using the commonly used drain-source voltage acceleration method where the device lifetime (Tau) is an exponential function of 1/Vds:

$$Tau = t_o \exp\left(\frac{B}{Vds}\right) \quad (3)$$

and t_0 and B are fit parameters. An additional advantage of the drain-source voltage acceleration method is that it can predict the maximum operating drain voltage for a given target device lifetime.

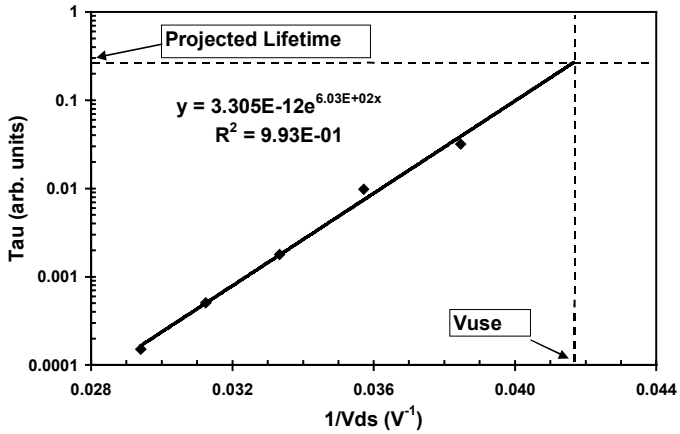


Figure 13. N-LDMOS (50 source array) Rdson device lifetime (Tau) plot vs. 1/Vds.

Array layout effects

Figure 5 showed that the initial N-LDMOS arrays failed to meet target HC lifetime requirements. Measurements and simulations show that modifying the N-LDMOS device layout can substantially improve HC performance. Figure 14 displays measured Rdson lifetime versus specific on-resistance (Rdson_sp) and source to drain layout spacing L (see Figure 1 for L definition) where:

$$\text{Rdson\_sp} = \text{Rdson} * \text{Array Area} \quad (4)$$

Figure 14 shows that increasing N-LDMOS layout spacing L by only 0.9 μm improves Rdson HC lifetime by over seven orders of magnitude. This HC lifetime improvement, though, is attained by increases in Rdson_sp and array area.

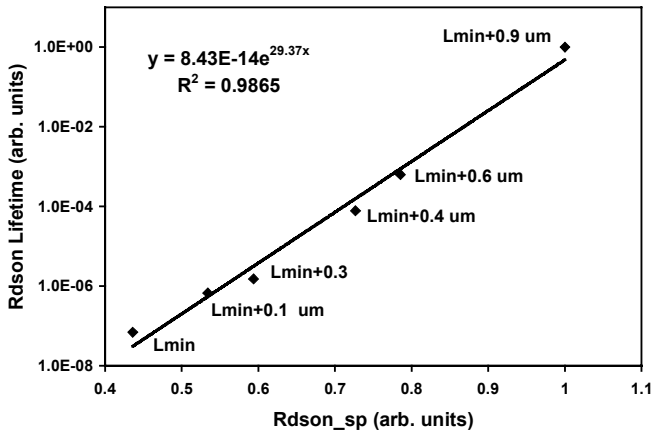


Figure 14. Rdson lifetime vs. Rdson_sp and N-LDMOS source to drain edge spacing L.

Figure 14 results can be understood by plotting simulated peak impact ionization rate versus Rdson lifetime as seen in Figure 15. Figure 15 shows to first order that a power law correlation exists between impact ionization rate and Rdson HC lifetime and that increasing the layout length L improves the HC lifetime. The driving force behind this improvement is a reduction in maximum electric field in the N-LDMOS extended drain region.

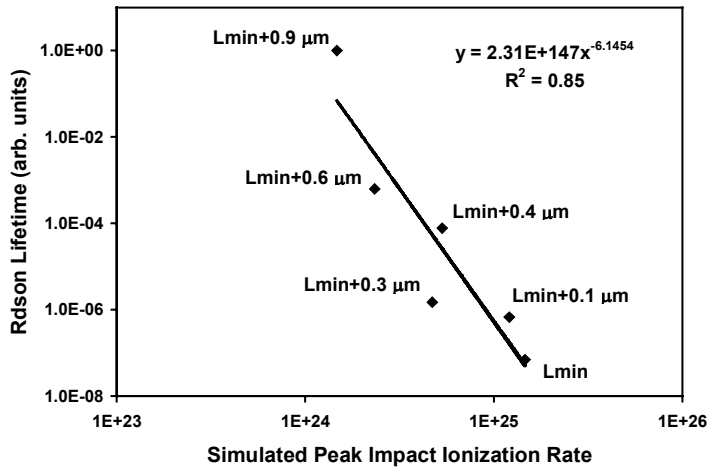


Figure 15. Simulated peak impact ionization rate vs. Rdson lifetime and N-LDMOS cell Size

SUMMARY AND CONCLUSIONS

Several key issues associated with N-LDMOS HC testing have been addressed. These include a qualitative understanding of device degradation results, validation of HC degradation and lifetime models and establishing the effect of device layout on HC lifetime. The results of this paper are summarized below:

- The HC degradation of linear drain resistance (Rdson) can be significant in N-LDMOS devices limiting the device useful operating voltage range.
- The HC performance of discrete (single source and drain) N-LDMOS devices does not scale to arrays.
- Increasing the device source to drain edge spacing significantly improves this device HC lifetime performance but with the tradeoff of increased Rdson and array area.
- Conventional NMOS degradation and lifetime models are valid for the N-LDMOS device.
- Simulation results and data strongly suggest that the N-LDMOS degradation mechanism is hot carrier generated interface states causing a build up of negative charge at the Si-FOX interface. This negative charge attracts holes depleting the negative charge in the extended drain region increasing Rdson.

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