DESIGN AND FPGA IMPLEMENTATION OF NON-SEPARABLE 2-D BIORTHOGONAL WAVELET TRANSFORMS FOR IMAGE/VIDEO CODING

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ABSTRACT

This paper reports on the design and hardware implementation of an efficient architecture for the non-separable 2-D discrete biorthogonal wavelet transforms (DBWT). The architecture adopts periodic symmetric extension at the image boundaries, therefore it conforms the JPEG-2000 standard. It computes the DBWT decomposition of an *NxN* image in approximately $2N^2/3$ clock cycles (ccs). Hardware implementation results based on a Xilinx Virtex-2000E FPGA chip showed that the processing of 2-D DBWT can be performed at 105 MHz providing a complete solution for the real-time computation of 2-D DBWT with image boundary handling.

1. INTRODUCTION

The 2-D Discrete Wavelet Transform (DWT) has taken the place at the forefront of research for the development of image and video processing applications. These wavelet based approaches have outperformed existing strategies in many areas including image denoising, segmentation and most notably compression. In 1992, Cohen, Daubechies and Feauveau established the theory of biorthogonal wavelet sytems [1]. Results have shown that biorthogonal wavelets offer improved coding gain, and produce less virtually detrimental artifacts when compressing at low bit rates than previous approaches such as the Discrete Cosine Transform (DCT), and for this reason biorthogonal wavelet based coding is being introduced into emerging standards such as JPEG 2000 [2]. Since the 2-D DWT requires an intensive amount of computation power, either the design of high-performance dedicated circuits or parallel systems is strategic for applications that require real-time performances.

Most of the effort towards the hardware architectures and implementations for the 2-D DWT has been concentrated on the separable orthonormal wavelet family, mostly based on the Recursive Pyramid Algorithm [3-4]. When the 2-D wavelet basis functions are separable, the 2-D DWT can be split into row-wise and column-wise 1-D operations. Whilst this approach produces predictable solutions, these architectures do not incorporate many aspects of 2-D processing.

The non-separable approach for computing the 2-D DWT consists of directly decomposing the input image into two dimensions. Only a few architectures [3,6] and just one hardware implementation [7] have been proposed for 2-D non-separable approach. A close examination of the non-separable approach enables following advantages to be identified:

- The non-separable architecture does not require any transposition. Therefore it avoids the latency and hardware area, which is $O(N^2)$, introduced by the transposer ;
- The use of non-separable 2-D filter directly instead of using 1-D filter units repetitively, simplifies control of the circuit and therefore leads to less circuit complexity (i.e. timing, routing etc.);
- When the wavelet basis functions are not separable, only the use of non-separable filter is possible. And, the non-separable filters provide more degrees of freedom in design, therefore leads to better filters.

In this paper, we propose a scalable VLSI architecture for the symmetrically extended non-separable 2-D biorthogonal wavelet transform. The architecture performs the decomposition of an *N*x*N* input image in $\approx 2N^2/3$ ccs. The symmetry/anti-symmetry properties of biorthogonal (linear-phase) filters have been exploited in order to further reduce VLSI-area. Performance results for the hardware implementations of a (9x7-tap) non-separable 2-D biorthogonal filter architecture on the Xilinx Virtex 2000E FPGA chip are presented.

The outline of this paper is as follows. In the next section, the non-separable 2-D DBWT is shortly recalled. The proposed architecture and its computing blocks are described in Section 3. FPGA implementations with performance results are presented in Section 4. Conclusions are summarised in Section 5.

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2. NON-SEPARABLE 2-D DISCRETE BIORTHOGONAL WAVELET TRANSFORMS

In the non-separable (or direct) approach, the decomposition is computed by four 2-D convolutions followed by a decimation by 2 in both horizontal and vertical directions as follows:

$$\begin{aligned} LL^j(m,n) &= \sum_{i=0}^{L-1}\sum_{k=0}^{M-1} ll(i,k)LL^{j-1}(2m-i,2n-k) \\ LH^j(m,n) &= \sum_{i=0}^{L-1}\sum_{k=0}^{M-1} lh(i,k)LH^{j-1}(2m-i,2n-k) \\ HL^j(m,n) &= \sum_{i=0}^{L-1}\sum_{k=0}^{M-1} hl(i,k)HL^{j-1}(2m-i,2n-k) \\ HH^j(m,n) &= \sum_{i=0}^{L-1}\sum_{k=0}^{M-1} hh(i,k)HH^{j-1}(2m-i,2n-k) \end{aligned} \quad (1)$$

where $ll(i,k)$, $lh(i,k)$, $hl(i,k)$ and $hh(i,k)$ are the coefficients of the low-low, low-high, high-low and high-high (LxM)-tap 2-D filter bases, respectively. $LL^j(m,n)$, $LH^j(m,n)$, $HL^j(m,n)$, and $HH^j(m,n)$ are the Low-Low, Low-High, High-Low and High-High subbands produced at the decomposition level j. As a special case, LL^{j-1} for j=1 represents the input image I.

In this paper, we focus our attention on biorthogonal filters. These filters are very attractive for implementing pyramidal structures since they do not require phase compensation between adjacent decomposition levels. Biorthogonal wavelet filters possess a linear-phase property and they have a symmetric (or anti-symmetric) impulse response. Their filter coefficients for a (LxM)-tap 2-D filter ($ll(i,k)$, $lh(i,k)$, $hl(i,k)$ and $hh(i,k)$) can thus be written as follows:

$$\begin{aligned} a_{\lceil L/2\rceil-i,\lceil M/2\rceil-j} &= \pm a_{\lceil L/2\rceil-i,\lceil M/2\rceil+j} = \\ a_{\lceil L/2\rceil+i,\lceil M/2\rceil-j} &= \pm a_{\lceil L/2\rceil+i,\lceil M/2\rceil+j} \end{aligned} \quad (2)$$

where $\lceil\ \rceil$ represents maximum integer and $i = 0,1,..,\lceil L/2\rceil$ and $j = 0,1,..,\lceil M/2\rceil$.

For the sake of illustration, the case of a (9x7-tap) biorthogonal filter (L=9 and M=7) will be considered in the rest of the paper. For an (9x7)-tap filter, the symmetry along with the rows of the filter (vertical symmetry) can be written as:

$$ll(4-i,k) = ll(4+i,k) \quad (3)$$

$[I]_{(2m-i)}$ and $[I]_{(2m+i)}$ rows adopt the same filter coefficients, therefore their point-wise summation can be processed together as:

$$\begin{aligned} LL^j_{\{0,8\}}(m,n) &= \sum_{i=0}^{8}\sum_{k=0}^{6} ll(0,k)\cdot\{LL^{j-1}(2m-8,2n-k) \\ &+ LL^{j-1}(2m,2n-k)\} \end{aligned} \quad (4)$$

where the subscript {0,8} correspond to the point-wise sum of the first and the ninth rows.

The center for horizontal symmetry is the fourth column and it is defined as:

$$ll(i,3-k) = ll(i,3+k) \quad (5)$$

which means that the $(3-i)^{th}$ and $(3+i)^{th}$ samples of point-wise sum of rows {0,8} are multiplied with the same filter coefficients. Therefore, the inner summation in Equation 4 becomes:

$$\begin{aligned} \underline{LL^j_{\{0,8\}}(n)} &= ll(0,3)\cdot x_{\{0,8\}}(2n-3) \\ &+ \sum_{i=0}^{2} ll(0,i)\cdot\{x_{\{0,8\}}(2n-6-i) + x_{\{0,8\}}(2n-i)\} \end{aligned} \quad (6)$$

where $x_{\{0,8\}}(n)$ represents the n^{th} element of the point-wise summation of the first and ninth rows.

3. THE NON-SEPARABLE 2-D DBWT ARCHITECTURE

3.1 Top-Level Architecture

The equations 4 and 6 can be mapped into the architecture for the (9x7) non-separable 2-D biorthogonal wavelet filter with three levels of decomposition (J=3) shown in Figure 1. The design of the non-separable 2-D discrete biorthogonal wavelet filter architecture has been derived from MRPA-liked based architecture in [6]. MRPA-liked based architecture exploits the down sampling of output sub-bands and perform the first decomposition level interspersed with all other levels by means of only one processing unit.

The architecture is composed of a set of $\lceil L/2\rceil = 5$ 1-D filter processors (P_i) and J sets of row delay circuits, R^j being used for the j^{th} level of decomposition where j=0,1,..,J. Each row-delay circuit R^j is composed of a pipe of (L-1) row-delay elements with $N=2^j$ memory cells. R^0 stores the rows of the input image while $R^j>0$ are used to store the rows of LL^j subband, which are used as input for computing the decomposition level j+1.

The even-numbered and odd-numbered rows of the input image are fed simultaneously into processors P_{2i} and P_{2i+1} in a word-serial fashion so that the decimated output can be directly computed. Computation of the different levels of decomposition is scheduled according to an algorithm that differs from the MRPA since the processors in this architecture require the parallel input of odd and even rows [6]. The k^{th} row of each subband at the decomposition level j, $[LL^j]_{2k}$ can only be computed when two adjacent rows from the previous level ($[LL^{(j-1)}]_{2k}$ and $[LL^{(j-1)}]_{2k+1}$) are produced and stored in $[R^{j-1}]_0$ and $[R^{j-1}]_1$. The rows LH^j , HL^j and HH^j are immediately output, while the row LL^j is fed back and stored either in $[R^j]_0$ if k is even or in $[R^j]_1$ if j is odd.

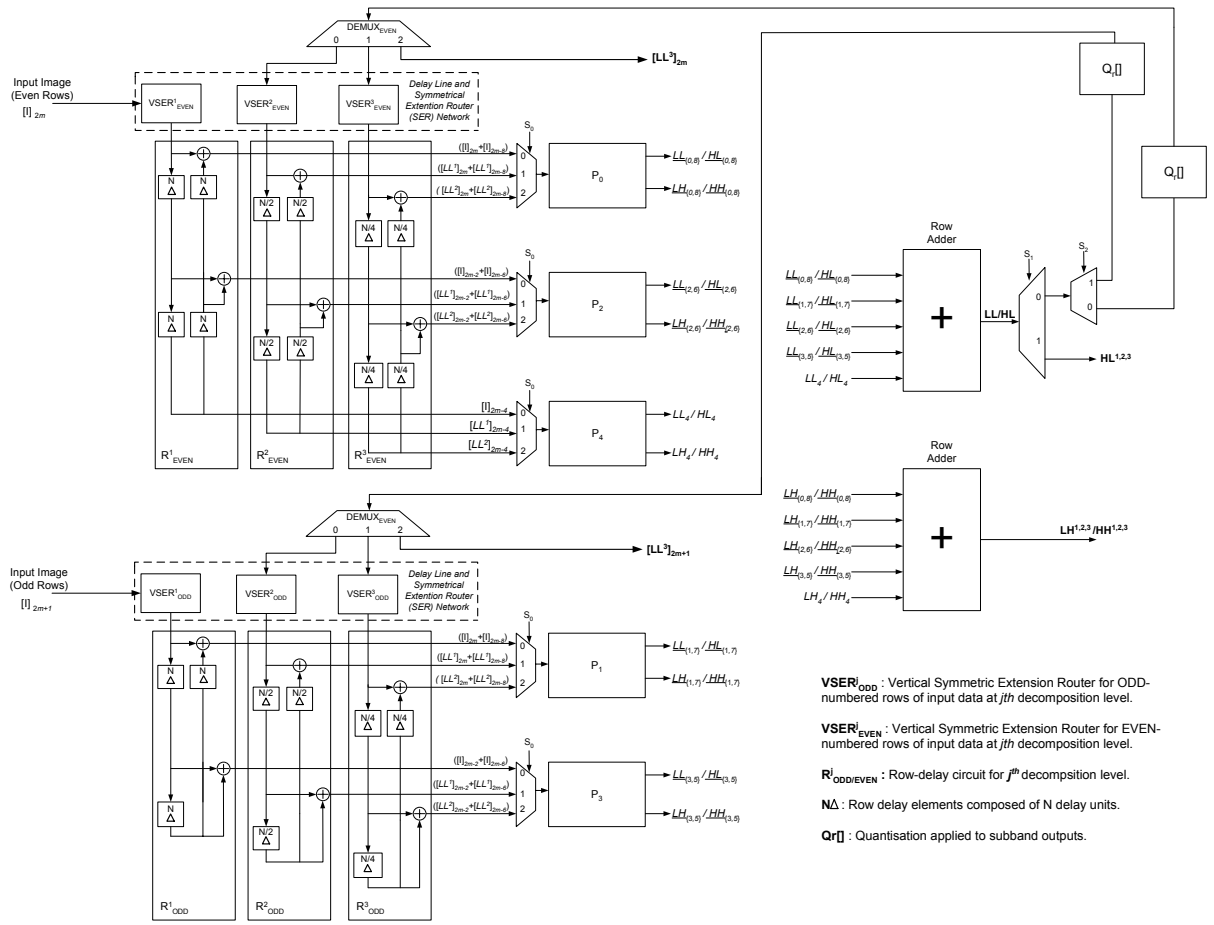

Figure 1 Non-separable (9x7)-tap 2-D DBWT top-level architecture.

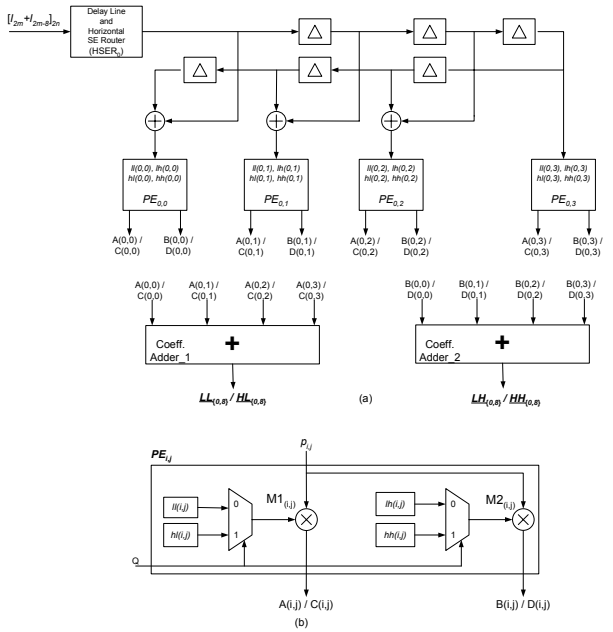

Figure 2 One-dimensional processor (P_0) and PE architecture where the filter length is M=7.

3.2. (1-D) Filter Processor

The number of (1-D) Filter processors has been reduced from L to $\lceil L/2 \rceil = 5$ by exploiting the symmetry property along rows of biorthogonal filters, as explained in Equation 4. For the considered (9x7)-tap 2-D filter, because of the symmetry along the fifth row of the filter kernel, relevant input rows (i.e. $[I]_0$ and $[I]_8$, $[I]_1$ and $[I]_7$) are added and then feed into associated processor (i.e. P_0, P_1) as shown in Figure 1.

Each processor P_i in the architecture is composed of a set of Processing Elements $PE_{(i,j)}$ and two coefficient adders as shown in Figure 2-a. The number of PEs has been reduced from M=7 to $\lceil M/2 \rceil = 4$ by exploiting the symmetry properties of (9x7)-tap biorthogonal filter along the fourth column. The relevant samples on the input row are added and connected to PE before the actual multiplication is performed.

Each PE consists of two multipliers (as shown in Figure 2-b). The multiplier $M1_{(i,j)}$ uses, in interleaved fashion controlled by the select signal Q, $ll(i,j)$ and $hl(i,j)$ and computes either $A(i,j)$ in even ccs and $C(i,j)$ in odd

ccs. Similary, $M2_{(i,j)}$ computes $B(i,j)$ and $D(i,j)$ by using $lh(i,j)$ and $hh(i,j)$ in even and odd ccs, respectively. Once these terms are computed, they are fed into coefficient adders in
the PEs (coeff._adder_1 and coeff._adder_2 in Figure2 - a), which produces 1-D decimated filter outputs.

Finally, these 1-D decimated filter outputs from each processor are fed into row-adders on the top-level (Figure 1) in order to produce *LL* and *LH* in even ccs and *HL* and *HH* in odd ccs. The *LL* output is recursively passed through the same filter according to the number of decomposition levels required.

3. Symmetric Extension

The symmetric extension of an input image is defined in JPEG-2000 standard [2]. The input image, according to non-separable approach, is extended by reflecting $\lceil L/2 \rceil$ rows to the up and down of the image, and $\lceil M/2 \rceil$ columns to the left and right of the image, where L and M are filter dimensions.

The vertical delay line and SER is basically composed of $\lceil L/2 \rceil$ number of row delay circuits for each level with $N/2^k$ delay elements. The SER handles the routing of extension rows along even and odd input lines. The vertical part of SE introduces a lag of $\lceil L/2 \rceil \cdot N$ ccs.

The extension of each input (1-D) row is managed by horizontal delay line and SER in each processor. The first $\lceil M/2 \rceil$ samples in each input row is delayed and then routed appropriately. The vertical part of SE introduces a lag of $\lceil M/2 \rceil$ ccs.

4. FPGA IMPLEMENTATION

In order to verify the performance of the proposed architecture, the non-separable 2-D biorthogonal wavelet filter designs have been ported to a Virtex-E2000 FPGA chip (package: bg560, speed grade 6) using a high-level hardware description language, Handel-C [8,9].

A 2's complement data format has been used in the implementations. The Handel-C model simulations showed that for a 9-bit input data wordlength, the wavelet coefficients from all levels are bounded by 2^{16}. Therefore, output data wordlength of 16 bits is enough to represent wavelet coefficients without causing any overflow. The internal wordlength accuracy of 25 bits is used. An internal quantization of 9-bit to the output is applied in order to avoid the growth of wordlength beyond 16 bits.

In this study, (9,7)-tap non-separable 2-D biorthogonal filters up to three levels of decomposition have been implemented. The embedded Block RAMs in the Virtex-E device have been used in order to implement row delay circuits (R_j). Table 1 shows implementation results, in terms of FPGA area occupied, maximum operating frequency (f_{max}) and computation time, for various decomposition levels for an input image size of N=512x512.

Table 1. FPGA implementation results on the Virtex-2000E chip for N=512x512.

Levels	Area (Slices)	Block RAMs	f_{max} (MHz)	Computation Time (ms)
1	3974 (%21)	14 (8%)	105	1
2	4126 (%22)	21 (13%)	97	3.2
3	4348 (%23)	28 (17%)	89	3.5

The proposed implementation presents a complete solution for the real-time computation of non-separable 2-D DBWT targeting image and video coding applications based on wavelets.

5. CONCLUSIONS

This paper reports on the design and FPGA implementation of an efficient architecture for the non-separable 2-D discrete biorthogonal wavelet transforms. The architecture is capable of performing the symmetrical extension at the image boundaries. It requires approximately $2N^2/3$ clock cycles (ccs) for the decomposition of an NxN image. FPGA implementation of a three-level of decomposition occupies only %23 of the Virtex-2000e FPGA chip and operates at 89MHz.

6. REFERENCES

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