PARALLEL INTERFERENCE CANCELLATION TECHNIQUE APPLIED TO DS-OCDMA SYSTEMS

Goursaud C., Julien-Vergonjanne A., Zouine Y., Aupetit-Berthelemot C., Cances J.P., and Dumas J.M.

UMOP/GESTE, CNRS FRE 2701, University of Limoges/ENSIL
Parc d'Ester BP 6804, 87 068 Limoges, FRANCE
phone: + (33) 5 55 42 36 70, fax: + (33) 5 55 42 36 80, email: goursaud@ensil.unilim.fr

ABSTRACT

This paper investigates the Parallel Interference Cancellation (PIC) with Hard Limiter technique in Direct Sequence Optical Code Division Multiple Access system (DS-OCDMA). The PIC technique consists of first estimating the interference by decoding all the non-desired users with a Conventional Correlation Receiver (CCR), and then of removing the estimated interference from the received signal in order to detect the desired user. We study an improvement of this technique: PIC+HL, in which we use an Hard Limiter (HL) before the CCR of the desired user, in order to limit the interference term due to the non-desired users bad cancellation. We develop the theoretical PIC+HL error probability expression from the PIC one in the chip synchronous case, for Optical Orthogonal Codes (OOC). We demonstrate that such receiver improves significantly the O-CDMA performances regards to conventional receivers.

1. INTRODUCTION

The CDMA method adapted from the cellular phone network has appeared from several years in the fiber-based optical networks as a multiple access solution for high-speed Local Area Networks (LANs). This technique called Optical Code Division Multiple Access (OCDMA) works by assigning to each user a specific code and could provide an asynchronous and simultaneous access to several users [1-6].

As incoherent optical CDMA systems require lower complexity than the coherent ones, they have been intensively studied. In such systems, the incoherent optical signal processing uses unipolar quasi-orthogonal codes. Thus the performances can be significantly reduced by Multiple Access Interference (MAI) as the number of active users increases.

In order to reduce the MAI impact, very long optical unipolar code sequences can be used. However, this requires a too large bandwidth regards to the speed limitations of encoding and correlating hardware. To reduce the code length and maintain good performances, one of the possible solutions is to mitigate the MAI by using an interference cancellation receiver. Several interference cancellation methods have appeared in the literature aiming at lowering the Bit Error Rate (BER) [4-6]. For example, a simple solution is the use of an optical Hard Limiter (HL) which removes some interference patterns [6].

But, in these cancellation techniques [4-6], the effect of MAI was not completely removed. We have presented in [7], a new interference cancellation receiver named Parallel Interference Canceller in the open literature (PIC)[8], which removes completely the MAI in some particular cases, and improves the system performances for the Optical Orthogonal Codes family (OOCs)[1].

In this paper, we present the PIC with an HL in front of the desired user receiver (PIC+HL). We develop the PIC+HL performances theoretical expression, and we prove that the PIC+HL outperforms the PIC receiver, and permits to reduce the code length in order to fit the speed limitations of encoding and decoding hardware.

2. THE DS-OCDMA SYSTEM

We consider an incoherent, synchronous Direct Sequence -Optical CDMA system (DS-OCDMA).

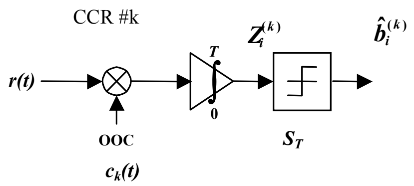

Fig 1 : The Conventional Correlation Receiver : CCR

Each user employs an on/off keying (OOK) modulation to transmit independent and equiprobable binary data upon an optical channel. A sequence code is impressed upon the binary data by the encoder. The sequence code is specific to each user, in order to be able to extract the data at the end receiver, by comparison with the sequence code.

The data spreading is realized with OOC[1]. These quasi orthogonal unipolar codes are defined by $(F, W, \lambda_a, \lambda_c)$ where F is the sequence length, and W the weight which corresponds to the number of "chip one" in the sequence. The auto and crosscorrelation constraints λ_a and λ_c are equal to one. The maximum number of users N in the OOC's class is defined as: $N = \lfloor (F-1)/W(W-1) \rfloor$.

We consider that noise contribution is less significant than MAI power, which is always the case in high loaded networks. So, the errors are only due to multi-user interference. At the receiver end, the electrical signal $r(t)$ is the sum of the users' signal: $r(t) = \sum_{j=1}^{N} b_i^{(j)} c_j(t)$

where $c_j(t)$ is the sequence code of the j^{th} user, and $b_i^{(j)} \in \{0,1\}$ is the i^{th} data bit of the j^{th} user. In a Conventional Correlation Receiver (CCR), the received signal $r(t)$ is multiplied by the code sequence corresponding to the desired user $c_k(t)$, and then the result is integrated (Fig. 1). We get the decision variable value $Z_i^{(k)}$:

$$\begin{aligned} Z_i^{(k)} &= \int_0^T r(t).c_k(t)dt \\ &= W.b_i^{(k)} + \sum_{j=1, j\neq k}^{N} b_i^{(j)}.\int_0^T c_k(t).c_j(t)dt \end{aligned} \quad (1)$$

The second term in (1) is the interference due to all the non-desired users (MAI). After that, the decision variable value is compared to the threshold level S_T and the estimation of the transmitted bit, $\hat{b}_i^{(k)}$, is given. Due to the codes unipolarity, errors can occur only when $b_i^{(k)}$ is a zero data and the MAI term is greater than the threshold level value S_T.

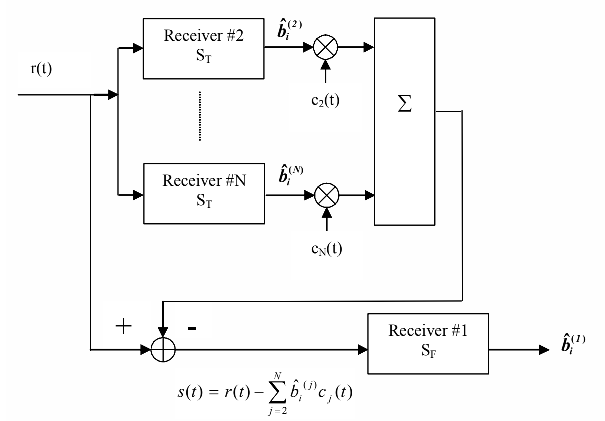

Fig 2 : Parallel interference cancellation structure

It has been shown [1] that the error probability P_{ES} for the ideal chip synchronous case is:

$$P_{ES} = \frac{1}{2} \sum_{i=S_T}^{N-1} \binom{N-1}{i} \left(\frac{W^2}{2F} \right)^i \left(1 - \frac{W^2}{2F} \right)^{N-1-i} \quad (2)$$

To improve the CCR performances, we can use an hard limiter (HL) [1,6]. This device clips the power to the chip power level during every chip interval T_c. It is defined by:

$$g(x) = \begin{cases} 0 & if \quad x < 1 \\ 1 & if \quad x \geq 1 \end{cases}$$

It has been shown [1] that the HL+CCR's error probability for the ideal chip synchronous case is:

$$P_{EHL} = 1/2 \binom{W}{S} \prod_{i=0}^{S-1} (1 - (1 - W^2/2F)^{N-1-i}) \quad (3)$$

3. PARALLEL INTERFERENCE CANCELLATION

3.1. Principles

A parallel interference cancellation structure aims at estimating the contributions of the non-desired users in order to remove it from the received signal. Thus, we can divide the structure in two main parts: the first one detects the $N-1$ non-desired users' data and removes the estimated contributions from the received signal, whereas the second part detects the desired user's data (fig 2).

3.2. PIC receiver

The first stage of Parallel Interference Cancellation receiver (PIC) is a parallel structure whose receivers are all CCRs. The signal applied to the second stage is expressed as :

$$s(t)=r(t)-\sum_{j=2}^{N}\hat{b}_i^{(j)}c_j(t)=b_i^{(1)}c_1(t)+\sum_{j=2}^{N}(b_i^{(j)}-\hat{b}_i^{(j)})c_j(t) \quad (4)$$

$(b_i^{(j)}-\hat{b}_i^{(j)})$ can take 2 values : "0" or "-1". So, the second term in (4) can generate either negative or null interference on user #1. Thus, errors can occur only when the desired user's sent datum is a 1, contrary to CCR. We have established in [7] that the theoretical expression of the PIC error probability is :

$$P_{EPIC}=(1/2)^N.\sum_{N_1=S_T-1}^{N-1}\sum_{N_2=W+1-S_F}^{N-1-N_1}\binom{N-1}{N_1}\binom{N-1-N_1}{N_2}(P_{IPIC})(1-P_{IPIC})^{N-1-N_1-N_2} \quad (5)$$

with $P_{IPIC}=W^2/F.\sum_{n_1=S_T-1}^{N_1}\binom{N_1}{n_1}\left(W^2/F\right)^{n_1}\left(1-W^2/F\right)^{N_1-n_1}$ (6)

where S_T $(0<S_T\le W)$ and S_F $(0<S_F\le W)$ are respectively the threshold levels of the non desired users' and the desired user' receiver. P_{IPIC} represents the probability for a non-desired user who sent a "0" to be an "interfering user", i.e. to create an interference of "-1" on user #1. A non-desired user is an interfering user if his datum is detected as a 1 instead of a 0, and if he has a chip in common with user #1.

3.3. PIC+HL receiver

In order to improve the PIC performances, we place an HL in front of the desired user's receiver. The aim of this HL is to mitigate the negative interferences due to the non desired users bad cancellation, on user #1. We call this receiver PIC+HL.

In order to analyze the PIC+HL performances, we develop the theoretical expression of its error probability $P_{EPIC+HL}$ for OOC $(F,W,1,1)$ and N simultaneous users.

The error probability can be written as:

$$P_{EPIC+HL}=\frac{1}{2}P(\hat{b}_i^{(1)}=1/b_i^{(1)}=0)+\frac{1}{2}P(\hat{b}_i^{(1)}=0/b_i^{(1)}=1)$$

As errors can occur only when the data sent is a "1", we consider that $b_i^{(1)}=1$. Moreover, we suppose that N_1 non-desired users sent a "1". In addition, among the remaining $N-1-N_1$ non desired users (who sent a "0"), we suppose that N_2 non desired users are interfering users. The probability to have this distribution D of N_1 non-desired users who sent a "1" and N_2 interfering users is :

$$P(D)=\binom{N-1}{N_1}(1/2)^{N_1}\times(1/2)^{N-1-N_1}\times\binom{N-1-N_1}{N_2}$$
$$=(1/2)^{N-1}\times\binom{N-1}{N_1}\times\binom{N-1-N_1}{N_2}$$

Thus

$$P_{EPIC+HL}=\frac{1}{2}\sum_{N_1=0}^{N-1}\sum_{N_2=0}^{N-1-N_1}P(D)\times P(\hat{b}_i^{(1)}=0/D\cap b_i^{(1)}=1)$$

So, we have to express $P(\hat{b}_i^{(1)}=0/D\cap b_i^{(1)}=1)$ for N_1 and N_2 given, i.e., we must determine the probability to have:

$$Z_i^{(1)}=\int_0^T c_1(t)\times g(r(t)-\sum_{j=2}^{N}\hat{b}_i^{(j)}c_j(t))dt$$
$$=\int_0^T c_1(t)\times g(c_1(t)+i(t))dt<S_F$$

We can first notice that $i(t)=\sum_{j=2}^{N}(b_i^{(j)}-\hat{b}_i^{(j)})c_j(t)dt$ is always negative or null. Indeed, with a CCR, there can be errors only when the data sent is a 0. In this case: $(b_i^{(j)}-\hat{b}_i^{(j)})=-1$. In the other cases, $(b_i^{(j)}-\hat{b}_i^{(j)})=0$.

Moreover, $i(t)$ lies between 0 and $-(N-1)$. However, due to the HL, $g(c_1(t)+i(t))$ can take only 2 values: 0 or 1. Thus, for a given τ, $g(c_1(\tau)+i(\tau))$ is equal to 1 only if $c_1(\tau)=1$ and $i(\tau)=0$. In the other cases, $g(c_1(\tau)+i(\tau))$ is null.

Consequently, in order to create an error, there must be at least $W-S_F+1$ different chips where $g(c_1(\tau)+i(\tau))=1$. This induces that at least $W-S_F+1$ non-desired users among N_2 must be interfering on at least $W-S_F+1$ different chips of user #1's code.

Thus, if $N_2<W-S_F+1$, we have $P(\hat{b}_i^{(1)}=0/D\cap b_i^{(1)}=1)=0$, there can not be error.

We have shown in [7] that, for a given N_1, when the receiver of the non-desired users is a CCR with a threshold level S_T, the probability for a non-desired user who sent a 0 to be an interfering user is:

$$P_I=W^2/F.\sum_{n_1=S_T-1}^{N_1}\binom{N_1}{n_1}\left(W^2/F\right)^{n_1}.\left(1-W^2/F\right)^{N_1-n_1}$$

This induces that if $N_1<S_T-1$, $P(\hat{b}_i^{(1)}=0/D\cap b_i^{(1)}=1)=0$ thus, there can not be error.

As the probability to have one interfering user is P_I, the probability to have N_2 interfering users among the $N-1-N_1$ users who sent a 0 is $(P_I)^{N_2} \times (1-P_I)^{N-1-N_1-N_2}$.

Having N_2 interfering users, there must be at least $W-S_F+1$ different chip overlapped, in order to create an error. There are $\binom{W}{W-S_F+1}$ possibilities of choosing $W-S_F+1$ chips among *W*. The probability for a chip to be overlapped by at least one user among N_2, is the complementary of the probability for a chip to be overlapped by none of the N_2 users. As the interfering users overlap one chip of user #1's code, the probability for an interfering user to overlap a chosen chip is $P_{Ichip} = 1/W$. Thus, a chosen chip is overlapped by at least one user among N_2 with the probability: $P_{chip\ with\ overlap} = 1 - \left(1 - 1/W\right)^{N_2}$

In addition to that, for the first chip studied, N_2 users can overlap. But, for the second chip, only $N_2 - 1$ users can overlap the second chip when the first chip is overlapped…

Thus, we get :

$$P(\hat{b}_i^{(1)} = 0 / D) = (P_I)^{N_2} (1-P_I)^{N-1-N_1-N_2} \times \binom{W}{W-S_F+1} \prod_{i=0}^{W-S_F} \left(1-(1-1/W)^{N_2-i}\right)$$

As it has been shown that there are no error if $N_1 < S_T - 1$ and $N_2 < W - S_F + 1$, the summation is realized from $S_T - 1$ up to $N-1$ for N_1, and from $W - S_F + 1$ up to $N-1-N_1$ for N_2. Thus, we finally get :

$$P_{EPIC+HL} = (1/2)^N . \sum_{N_1=S_T-1}^{N-1} \sum_{N_2=W+1-S_F}^{N-1-N_1} \binom{W}{W-S_F+1} \prod_{i=0}^{W-S_F} \left(1-(1-1/W)^{N_2-i}\right) \times \binom{N-1}{N_1} \binom{N-1-N_1}{N_2} (P_I)^{N_2} (1-P_I)^{N-1-N_1-N_2} \quad (7)$$

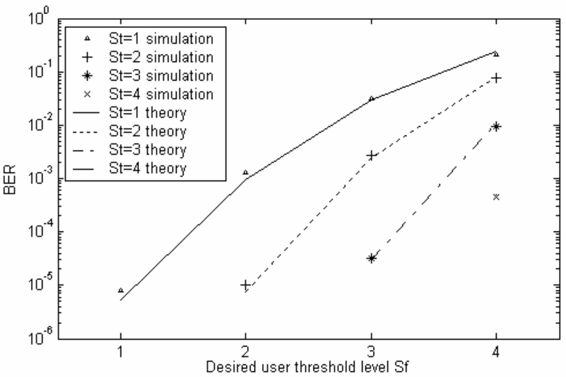

Fig 3 : Equation (5) validation with OOC(64,4) with N=5

4. NUMERICAL RESULTS ANALYSIS

4.1. Validation of the theoretical analysis

Considering the theoretical expressions (5) and (7), we can note that for both PIC and PIC+HL, if $W+1-S_F > N-S_T$, there will be no term in the equations (5) and (7)'s summation.

Thus, there is no error if the following inequality is verified:

$$W + 1 - S_F + S_T > N \quad (8)$$

In order to validate our theoretical expression, we plotted on fig. 3 the comparison between theoretical and simulated results for $P_{EPIC+HL}$. The error probability is plotted versus the threshold values for respectively S_F and S_T of the desired and non-desired users' CCR, for a *(F=64,W=4)* OOC's with *N=5* users.

We can first point out that the theoretical results fit with simulation results, thus, we can consider that the expression (7) correctly describes the PIC+HL receiver's performances.

In addition, we can notice missing points on the curves. All the missing points *((S_T =2, S_F =1), (S_T =3, S_F =1), (S_T =3, S_F =2), (S_T =4, S_F =1), (S_T =4, S_F =2), (S_T =4, S_F =3))* correspond to a null error probability and are defined by the inequality (8). Moreover, we can extrapolate from the curves evolution that the optimal threshold level set is *(S_T=W,S_F=1).*

As the theoretical expression (7) describes correctly the PIC+HL receiver performances, we use this theoretical expression for the performances study.

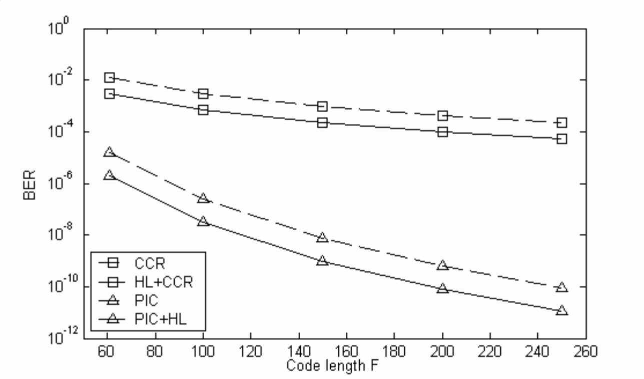

Fig 4 : PIC+HL performances for OOC(F,3) with N=20

N	10	20	30
CCR	17000	37000	55000
HL+CCR	10000	22000	40000
PIC	200	480	800
PIC+HL	150	370	600

Table I :Minimal code length required for BER<10^{-9} for W=3.

4.2. Results

We show the PIC+HL performances as a function of one of the OOC parameters: the code length *F*. We plot, on fig 4, the theoretical performances of the CCR (2), the HL+CCR (3), the PIC (5) and the PIC+HL (7) as a function of *F*, for *W=3, N=20*. We consider the optimal threshold levels for these receivers, i.e. for the CCR and the HL+CCR : *S=W*, and for the PIC and the PIC+HL : $S_F=1$ and $S_T=W$.
We can observe that the PIC+HL receiver performances are better than the other receivers' ones. Moreover, the variation of a parameter induces the same impact on the performances: we can verify for all the receivers that the BER decreases when the code length *F* increases.
In order to estimate the benefit of the PIC+HL for the OOC parameters, we have evaluated in Table I the minimal code length *F* as a function of the number of users for *W=3,* for the different receivers to obtain the BER value required in optical networks, i.e : 10^{-9}.
We can observe that for a given code weight, the minimal code length required for a BER lower or equal than 10^{-9} is smaller with the PIC+HL than with the other receivers.
In realistic systems, the chip rate is upper-bounded by the hardware speed limitation. Thus, with an efficient receiver as PIC or PIC+HL, we can relax the constraint on code length, thus on the chip rate, in order to realize realistic O-CDMA systems.

5. CONCLUSION

An interference cancellation method applied to Optical CDMA system has been investigated by using a parallel receiver scheme with hard limiter, called PIC+HL. The theoretical expression of the error probability in the case of Optical Orthogonal Codes has been established. It has been theoretically demonstrated that under specific conditions between the code parameters and the number of users, the interference due to non desired users could be totally neutralized.

From numerical calculation and simulation, we have proofed the reliability of the theoretical analysis. We have illustrated with a study as a function of one of code parameters (code length), that the proposed scheme performances outperform the ones of conventional receivers. This is confirmed by a complete parametric study that we have performed. Moreover, we have shown that, thanks to its good performances, the PIC+HL permits either to improve the performances, or to reduce the code length. The advantage of such a receiver is to reduce the required hardware bandwidth, in order to approach workable systems.

6. REFERENCES

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