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A Survey on Synthesis of Resistive n-port Networks

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Abstract— **A survey on the development of resistive network synthesis is presented. Tellegen's result is first introduced, which shows that paramountcy is the necessary and sufficient condition for synthesis if $n \leq 3$. Then, some more general cases are presented, including works by Cederbaum, Guillemin, Brown, Reed, Weinberg, and Boesch. These results range from necessary realizability conditions of general resistive n-port networks to realizability conditions of a subclass of such networks, which are mostly based on graph theory. Recently, there has been some new development on the realization of resistive n-port networks containing $2n$ terminals, motivated by mechanical network synthesis using the element extraction method.**

I. INTRODUCTION

Passive network synthesis is an important subject in circuit theory, which has experienced a golden era in the 1930s–1970s. The most general and well-known transformerless realization approach, the Bott-Duffin procedure [1], yields a large number of redundant elements. Until now, the minimal realization problem of a passive one-port network without transformers has not been fully solved even for lower-order functions. For a passive n-port network, it is known that the immittance matrix must be positive real, and conversely any positive-real matrix is realizable with a finite number of resistors, capacitors, inductors, and transformers [2]. However, the transformerless RLC realization for $n \geq 2$ is still an open and challenging problem. After the 1970s, the research interest in passive network synthesis has declined partially due to the development of integrated circuits.

Recently, a new mechanical element named "inerter" [3], [4] has been introduced, which can enhance performances of mechanical systems [4]. More importantly, the inerter completes the analogy between passive mechanical systems and electrical ones. Therefore, the theory of passive network synthesis can be applied to design mechanical systems, making mechanical design more systematic. As a consequence, the research of passive network synthesis has been revived, and a series of new results in this area have appeared in the past few years [4]–[12]. In particular, there is an independent call for a renewed investigation by Kalman [13].

A resistive n-port network is a circuit consisting of only passive resistors, whose realizability problem has been an important topic in the field of passive network synthesis. The realization of resistive n-port networks is a critical step towards the synthesis of RLC n-port networks. Through analogy, the realizability of n-port networks containing other one-kind-of-elements can be directly obtained. Moreover, the minimal realization of one-port networks can be converted to the synthesis of resistive n-port networks by elements extraction [6], [8], [9]. However, the investigation on the synthesis of resistive n-port networks still has a long way to go, where only the case of $n \leq 3$ and the realization of admittances with $n+1$ terminals have been solved.

This paper will give a brief review of the investigations on resistive n-port networks from the 1950s to the 1970s [14]–[48] and introduce some recent results on this topic obtained in [12]. The investigation on this topic starts from Tellegen's work in 1952, which discusses the realization problems of resistive two-port and three-port networks. Then, many researchers continued to investigate the general properties of resistive n-port networks. By 1965, the realization problem of the admittance for resistive n-port networks with $n+1$ terminals had been solved. Since then, most of the works focused on realizations with more than $n+1$ terminals. However, it should be noted that the realizability conditions of the impedance and admittance of resistive n-port networks when $n > 3$ are not the same, and that attempts on realizations of impedances are much fewer than those of admittances.

The remaining part of this paper is organized as follows. Section II lists the main notations used in this paper. Section III discusses the realizability problem of two-port and three-port resistive networks. In Section IV, investigations on general n-port networks are reviewed. Section V introduces the realization of the admittance matrices of resistive n-port networks containing $n+1$ terminals. Section VI reviews the investigation on the realization problem of resistive n-port networks containing more than $n+1$ terminals. In Section VII, some recent results are reported. Conclusion is drawn in Section VIII.

II. NOTATIONS

Denote an *augmented graph*, *port graph*, and *network graph* by $\mathcal{G}$, $\mathcal{G}_p$, and $\mathcal{G}_e$, respectively, where $\mathcal{G} = \mathcal{G}_p \cup \mathcal{G}_e$. $\mathcal{T}$ denotes a tree of $\mathcal{G}$, $\mathcal{G}_{pt}$ denotes the port graph that is also a tree of $\mathcal{G}$, and $\mathcal{G}_{ec}$ denotes the network graph that is also a complete graph. The *fundamental cut-set matrix* and *fundamental circuit matrix* are respectively denoted by Q_f and B_f. I_n denotes the unit matrix of order n, and $E_{n,m}$ denotes the matrix consisting of the first m columns of I_n. W and L respectively denote submatrices of Q_f and

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B_f corresponding to $\mathcal{G}_e$. The vectors of port currents and voltages are denoted by $\hat{I}$ and $\hat{V}$. Denote the vectors of element currents and voltages by $\hat{J}$ and $\hat{U}$. G (D) denotes the diagonal element admittance (impedance) matrix, which is the diagonal matrix whose diagonal entries are admittances of the elements of the n-port network. Moreover, denote admittance and impedance matrix of the n-port network by Y_n and Z_n, and R denotes the impedances of two-port and three-port networks. $\mathfrak{W}_{ij}$ denotes the *tree transformation matrix* from $\mathcal{G}_{pt_i}$ to $\mathcal{G}_{pt_j}$. The symbol $\dotplus$ denotes the direct sum of two matrices. $\mathbb{S}^n$ denotes the set of real symmetric $n \times n$ matrices. Some of the results are based on classical graph theory [49], [50].

III. REALIZABILITY FOR $n \leq 3$

This section briefly reviews the proof [5, Appendix A] of Tellegen's work [14], where the realizability problems of resistive two-port and three-port networks are solved. The definition of paramountcy, one of the most important concepts in the synthesis of resistive n-port networks, is presented as follows.

Definition 1: [15] A real symmetric matrix is *paramount* if each of its principal minors is not less than the absolute value of any other minor built from the same rows.

The *cross-sign change* of a matrix is defined as follows.

Definition 2: [16] A *cross-sign change* of a matrix is to change the sign of each non-zero entry in the ith row and ith column.

It is shown in [51] that the absolute value of the voltage v (or current i) applied at two terminals of a resistive network cannot be less than any other response voltages (or currents). Utilizing this result, [5, Appendix A] shows that the impedance $R \in \mathbb{S}^2$ of the resistive two-port network must be paramount. Conversely, any paramount impedance $R \in \mathbb{S}^2$ is realizable by one of the resistive two-port networks shown in Fig. 1. More generally, through applying the current generator at any port and properly open- or short-circuiting the other two, it can be shown that the impedance $R \in \mathbb{S}^3$ of the resistive three-port network must also be paramount. To show the converse, it suffices to prove that any paramount matrix $R \in \mathbb{S}^3$ can be realized by the network shown in Fig. 2 with non-negative elements after a finite number of cross-sign changes and a proper rearrangement of rows and columns. A cross-sign change of the impedance (or admittance) means switching the polarity at a port, and exchanging two rows and corresponding columns means swapping two ports. The detail of the derivation is referred to [5, Appendix A]. Since the augmented graphs of these realizations in Figs. 1 and 2 are planar, the realizability of the admittance can be similarly discussed by the principle of duality. As a summary, the following theorem is obtained.

Theorem 1: [5], [14] Paramountcy is a necessary and sufficient condition for any second- or third-order real symmetric matrix to be realizable as the impedance (or admittance) of a two- or three-port network.

It means that the realizability problem of resistive n-port networks when $n \leq 3$ has been solved.

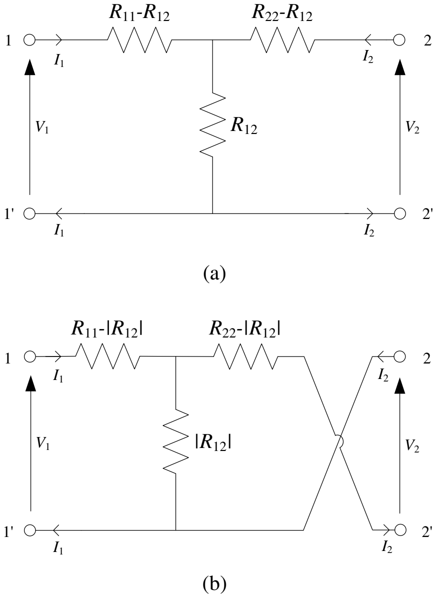


Fig. 1. The circuits for the realization of resistive two-port networks [5], where (a) corresponds to the case of $R_{12} \geq 0$, and (b) to $R_{12} < 0$.

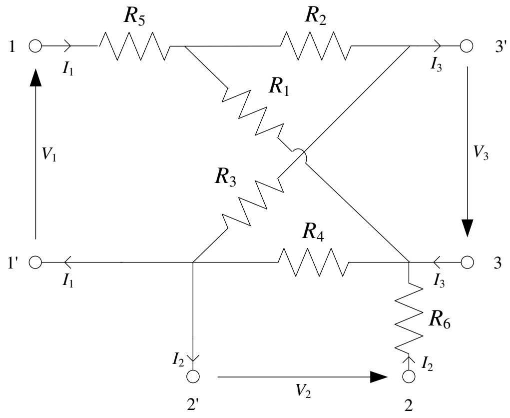


Fig. 2. The circuit for the realization of resistive three-port networks [5].

IV. GENERAL PROPERTIES OF RESISTIVE n-PORTS

Beyond the case of $n \leq 3$, the synthesis of n-port resistive networks for $n > 3$ needs to be further investigated. In this section, several general properties of resistive n-port networks are presented. It is known that both the admittance and impedance matrices of the resistive n-port network are positive definite because of its passivity and reciprocity [2]. However, additional conditions are needed due to the fact that transformers are not present. Based on graph theory, Cederbaum showed that the admittance (or impedance) matrix of the resistive n-port network is necessarily paramount [17], which is in general a subset of the original necessary conditions given in [18]. Before a brief overview of his derivation, an important concept is introduced below.

Definition 3: [17], [49] A matrix having all its subdeterminants equal to ± 1 or 0 is called an *E-matrix*.

Without loss of generality, it is assumed in [17] that the network graph $\mathcal{G}_e$ is connected and contains all the v vertices of the augmented graph $\mathcal{G}$, and the port graph $\mathcal{G}_p$ is part of a tree $\mathcal{T}$ of $\mathcal{G}$. Suppose that Q_f is the fundamental cut-set matrix of $\mathcal{G}$, expressed as $Q_f = [I_{v-1}, M] = [E_{v-1,n}, W]$, whose first n columns correspond to the edges of $\mathcal{G}_p$. Then, we can imply that the impedance Z_n is the first $n \times n$ principal submatrix of $(WGW^{\mathrm{T}})^{-1}$, where WGW^{T} must be nonsingular by the assumption. As discussed in [17], W must be an E-matrix, which implies that WGW^{T} must be a paramount matrix based on the Binet-Cauchy theorem [52]. Therefore, Z_n must be paramount, since the inverse of a nonsingular paramount matrix must be paramount by Jacobi's theorem [52]. Similarly, the discussion can be applied to admittance Y_n of the resistive n-port network. It is known that Y_n can be expressed as the first $n \times n$ principal submatrix of $Y_n = (LDL^{\mathrm{T}})^{-1}$, where $D \in \mathbb{R}^{e \times e}$ is the diagonal element impedance matrix, and L is the submatrix of the basic circuit matrix $B_f = [I_{e+n-v+1}, X] = [E_{e+n-v+1,n}, L]$, whose first n columns correspond to the edges of $\mathcal{G}_p$. Since L is an E-matrix, Z_n must be paramount. As a summary, the following theorem is obtained by Cederbaum [17].

Theorem 2: [17] If a symmetrical matrix $Y_n \in \mathbb{S}^n$ (or $Z_n \in \mathbb{S}^n$) is the admittance (or impedance) of the resistive n-port network, then Y_n (or Z_n) must be paramount.

Cederbaum's mild assumption [17] guarantees that WGW^{T} (or LDL^{T}) must exist and be nonsingular. However, when there exists a circuit in $\mathcal{G}_p$, WGW^{T} does not exist because of the nonexistence of $Q_f = [E_{v-1,n}, W]$, whose first n columns correspond to the edges of $\mathcal{G}_p$. An alternative proof of Theorem 2 is presented by Bruno and Weinberg [19], which is based on an alternative formula for the admittance and impedance of resistive n-port networks [20] and can handle the case of nonexistence of WGW^{T} (or LDL^{T}).

Theorem 3: [20] If the admittance Y_n of a resistive n-port network exists, then it can be written as

$$Y_n = B_{f2}^{\mathrm{T}}(B_{f1}DB_{f1}^{\mathrm{T}})^{-1}B_{f2}, \tag{1}$$

where D is the diagonal element impedance matrix, and B_{f1} and B_{f2} constitute the fundamental circuit matrix $B_f = [B_{f1}, B_{f2}]$ of $\mathcal{G}$ with the columns of $B_{f1} = [I_{e+n-v+1}, B_{f12}]$ corresponding to the edges of $\mathcal{G}_e$. If the impedance Z_n of a resistive n-port network exists, then it can be written as

$$Z_n = Q_{f2}^{\mathrm{T}}(Q_{f1}GQ_{f1}^{\mathrm{T}})^{-1}Q_{f2}, \tag{2}$$

where G is the diagonal element admittance matrix, and Q_{f1} and Q_{f2} constitute the fundamental cut-set matrix $Q_f = [Q_{f1}, Q_{f2}]$ of $\mathcal{G}$ with the columns of $Q_{f1} = [I_{v-1}, Q_{f12}]$ corresponding to the edges of $\mathcal{G}_e$.

Remark 1: $B_{f1}DB_{f1}^{\mathrm{T}}$ (or $Q_{f2}GQ_{f2}^{\mathrm{T}}$) is always nonsingular if and only if Y_n (or Z_n) exists [20].

Remark 2: The admittance of a resistive n-port network with $n+1$ terminals (no internal nodes) can be expressed as

$$Y_n = WGW^{\mathrm{T}}, \tag{3}$$

where $[I_n, W]$ is the fundamental cut-set matrix of $\mathcal{G}$. The impedance of a resistive n-port network with n independent circuit can be expressed as

$$Z_n = LDL^{\mathrm{T}}, \tag{4}$$

where $[I_n, L]$ is the fundamental circuit matrix of $\mathcal{G}$.

As a consequence, [19] shows that Y_n and Z_n as in (1) and (2) must be paramount through the Binet-Cauchy theorem [52], which also proves Theorem 2. To show the paramountcy both the proofs in [17] and [19] make use of the property of the E-matrix and some conclusions of linear algebra such as the Binet-Cauchy theorem. The main difference is the formula of the impedance (or admittance) used.

Making use of paramountcy, [21] generalizes Talbot's result in [51] to the vector case: if excitation voltages $\hat{V}_1 \in \mathbb{R}^k$ (or currents $\hat{I}_1 \in \mathbb{R}^k$) are applied to k ports of a resistive n-port network, and $\hat{V}_2 \in \mathbb{R}^k$ (or currents $\hat{I}_2 \in \mathbb{R}^k$) are voltages (or currents) of any other k ports (or elements), then the determinant and all the subdeterminants of the matrix $B \in \mathbb{R}^{k \times k}$ satisfying $\hat{V}_2 = B\hat{V}_1$ (or $\hat{I}_2 = B\hat{I}_1$) do not exceed unity. In [22], the realization properties of the admittance (or impedance) matrix with irreducible diagonal entries are investigated. Topological properties of realizations are first shown for the admittance Y_n and impedance Z_n with a diagonal entry equal to at least one off-diagonal entry of the same row. The diagonal entry cannot be further reduced because of the constraint of paramountcy. Furthermore, the following necessary condition is obtained.

Theorem 4: [22] If an admittance $Y_n \in \mathbb{S}^n$ (or impedance $Z_n \in \mathbb{S}^n$) with all the diagonal entries respectively equal to a row of entries can be realized by the resistive n-port network, then Y_n (or Z_n) is realizable with $n+1$ terminals (or with n independent circuits).

Making use of Theorem 4, Cederbaum presented a paramount matrix [22] that can be realized as neither the impedance nor the admittance of the resistive n-port network, which means that paramountcy is not always a sufficient condition for realization when $n > 3$. In addition, by constructing another matrix, [22] also shows that the realizability conditions of the admittance and impedance of the resistive n-port network are not the same for $n > 3$. References [23], [24] also discuss the difference between the admittance and impedance realizability conditions. Reference [25] alternatively shows that paramountcy is not sufficient, where new criteria guaranteeing the non-realizability of an irreducible paramount matrix are presented.

V. REALIZABILITY OF ADMITTANCES WITH $n+1$ TERMINALS

The realizability problem for any symmetric matrix $Y_n \in \mathbb{S}^n$ as the admittance of resistive n-port networks containing $n+1$ terminals has been solved. This section briefly reviews this subject. It is known that the generalized star-mesh transform [26] can eliminate internal nodes of the n-port resistive network. It is assumed in the rest of this paper that all the nodes of a resistive n-port network must be terminals.

The realization problem of resistive n-port networks with $n+1$ terminals was first investigated by Cederbaum in [27]. It is known that the admittance of such a class of networks is necessarily written as the unimodular congruence $Y_n = AGA^{\mathrm{T}}$, where $A \in \mathbb{R}^{n\times e}$ is an E-matrix and $G \in \mathbb{R}^{e\times e}$ is a diagonal matrix with all positive entries. Reference [27] establishes a direct algebraic procedure for decomposing any $Y_n \in \mathbb{S}^n$ into the unimodular congruence form. The procedure can either yield an essentially unique decomposition or show that the decomposition is impossible. After obtaining the matrices A and G, the technique suggested by Guillemin [28] or the Gould algorithm [53] can be utilized for the final realization. It should be noted that the method by Cederbaum also applies to the realization of the impedance as the resistive n-port network containing n independent circuits. However, the disadvantage of this method is that one has to check the realizability of a given matrix by proceeding the decomposition and the final realization procedure. This will be very complex for many cases. Therefore, more straightforward methods are needed.

After the pioneering work of Cederbaum, Brown *et al.* [16], [29], [30], [31] have successfully derived necessary and sufficient conditions for the realizability of such a class of networks as well as formulas of the elements, which are only in terms of entries of the admittance. The methodology is to establish the relationship between the entries of the matrix and the values of the involved elements. The condition then follows from the constraint that the elements are non-negative. To better introduce their works, some definitions are presented as follows.

Definition 4: [50] A connected graph in which between each pair of vertices there exists one and only one edge is called a *complete graph* (see Fig. 3).

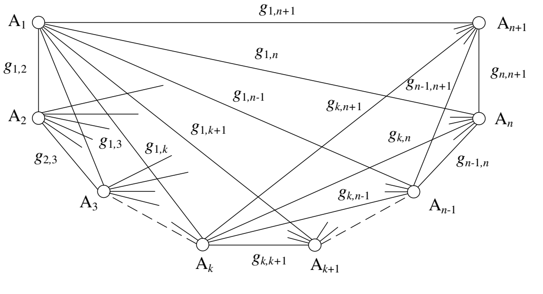
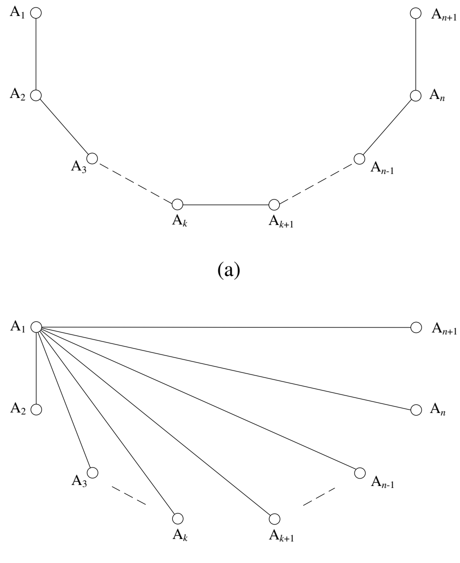


Fig. 3. The complete graph containing $n+1$ vertices (see [30]).

Definition 5: [30] A tree in which there are at most two edges incident to each vertex is called a *path tree* (see Fig. 4(a)). A tree in which each branch is incident to a common vertex is called a *Lagrangian tree* (see Fig. 4(b)).

Definition 6: [32] A *dominant matrix* is a real symmetric matrix such that each of its main diagonal entries is not less than the sum of the absolute values of all other entries in the same row.

Definition 7: [32] An nth-order *uniformly tapered matrix* is a real symmetric matrix with entries satisfying $y_{ij} - y_{i,j+1} \geq y_{i-1,j} - y_{i-1,j+1}$ for $j \geq i$, where $y_{0,i} = y_{j,n+1} = 0$ for all $i, j = 1, 2, ..., n$.



(a)

(b)

Fig. 4. Graphs of (a) path tree and (b) Lagrangian tree containing $n+1$ vertices (see [30]).

For the investigation of resistive n-port networks with $n+1$ terminals, it is assumed in [16], [30], [31] that the network graph is a complete graph with each edge corresponding to a non-negative element. Besides, the port graph is also a tree of $\mathcal{G}$. In order to distinguish the $(n+1)$-terminal case with more general ones, denote the network graph and port graph as $\mathcal{G}_{ec}$ and $\mathcal{G}_{pt}$, respectively. It is clear that augmented graph $\mathcal{G}$ satisfies $\mathcal{G} = \mathcal{G}_{pt} \cup \mathcal{G}_{ec}$. From Remark 2, it follows that the admittance Y_n can be expressed in the form of (3), where W is the fundamental cut-set matrix of $\mathcal{G}_{ec}$. It implies that the admittance of each element g_{ij} can be linearly and uniquely expressed in terms of entries of Y_n, when $\mathcal{G}_{ec}$ and $\mathcal{G}_{pt}$ including their orientations are fixed. As shown in [16], changing the orientation of any edge in $\mathcal{G}_{ec}$ does not affect Y_n, and changing the orientation of an edge in $\mathcal{G}_{ec}$ corresponds to a cross-sign change of Y_n. It is also shown in [31] that any real symmetric matrix can be regarded as the admittance of the graph $\mathcal{G} = \mathcal{G}_{pt} \cup \mathcal{G}_{ec}$, where $\mathcal{G}_e$ may correspond to negative elements. Therefore, in order to solve the realizability problem, it suffices to find conditions such that the values of the elements are non-negative. In [30], the values of the elements are expressed in terms of the entries of Y_n when $\mathcal{G}_{pt}$ is a path tree and the Lagrangian tree, respectively. Then, the following theorem follows.

Theorem 5: [29], [30] A matrix $Y_n \in \mathbb{S}^n$ can be realized as the admittance of the resistive n-port network with $n+1$ terminals, whose port graph $\mathcal{G}_{pt}$ is a path tree, if and only if after a finite number of cross-sign changes and a proper rearrangement of rows and columns Y_n is a uniformly tapered matrix. Specially, when $\mathcal{G}_{pt}$ is a linear and ordered tree (see [12]), no cross-sign change or rearrangement of rows and columns is needed, where the ports are assumed to be numbered corresponding to the rows (columns) of the matrix.

Theorem 6: [29], [30] A matrix $Y_n \in \mathbb{S}^n$ can be realized as the admittance of a resistive n-port network with $n+1$ terminals, whose port graph $\mathcal{G}_{pt}$ is a Lagrangian tree, if and only if after a finite number of cross-sign changes Y_n is a dominant matrix with all the off-diagonal entries non-positive. Specially, when all the edges of $\mathcal{G}_{pt}$ oriented from or toward the common vertex, no cross-sign change or rearrangement of rows and columns is needed.

For the realizability of networks with other kinds of port graphs, it suffices to convert them into the network with a path tree or a Lagrangian tree. The concept of the *tree transformation matrix* is presented as follows.

Definition 8: [31] Consider a graph $\mathcal{P} = \mathcal{G}_{pt_i} \cup \mathcal{G}_{pt_j}$ with $n+1$ vertices, where $\mathcal{G}_{pt_i}$ and $\mathcal{G}_{pt_j}$ are both $(n+1)$-vertex trees. Let $[I_n, \mathfrak{W}_{ij}]$ be a fundamental cut-set matrix of $\mathcal{P}$, where columns of I_n correspond to $\mathcal{G}_{pt_j}$ and columns of $\mathfrak{W}_{ij}$ correspond to $\mathcal{G}_{pt_i}$. Then, $\mathfrak{W}_{ij}$ is called the *tree transformation matrix* from $\mathcal{G}_{pt_i}$ to $\mathcal{G}_{pt_j}$.

The tree transformation matrix satisfies the following important property.

Theorem 7: [31] For graphs $\mathcal{G}_i = \mathcal{G}_{pt_i} \cup \mathcal{G}_e$ and $\mathcal{G}_j = \mathcal{G}_{pt_j} \cup \mathcal{G}_e$, whose fundamental cut-set matrices are $[I_n, W_i]$ and $[I_n, W_j]$, respectively, the following relation is satisfied: $W_j = \mathfrak{W}_{ij} W_i$.

Therefore, it is clear that Y_n is realizable by a resistive n-port network whose port graph is $\mathcal{G}_{pt_i}$ if and only if $\mathfrak{W}_{ij} Y_n \mathfrak{W}_{ij}^{\mathrm{T}}$ is realizable by the one with port graph $\mathcal{G}_{pt_j}$. Letting $\mathcal{G}_{pt_j}$ denote the Lagrangian tree $\mathcal{G}_{pt_L}$ whose edges are all oriented from or toward the common vertex. Together with Theorem 6, a necessary and sufficient condition is obtained for the realizability of the resistive n-port network with $n+1$ terminals, which is stated as follows.

Theorem 8: [31] A matrix $Y_n \in \mathbb{S}^n$ is realizable as the admittance of a resistive n-port network containing $n+1$ terminals whose directed port graph is $\mathcal{G}_{pt_i}$, if and only if there exists $\mathfrak{W}_{iL}$ such that $\mathfrak{W}_{iL} Y_n \mathfrak{W}_{iL}^{\mathrm{T}}$ is a dominant matrix with all the off-diagonal entries being non-positive.

Since the number of port graphs containing $n+1$ vertices must be finite, Theorem 8 can be utilized to test the realizability of any given matrix by enumerating all the possible graphs. However, the workload may be very large especially for large n. Guillemin [29] first considered determining the possible port graphs of the realization from admittance Y_n. Later, Biorci and Civalleri [33] proposed a topological solution to such a problem, which is simpler and quicker. Through establishing a series of conclusions that relate the properties of a port graph to the *sign matrix* S_n [34] or to the absolute values of the off-diagonal entries, a unified procedure is developed, which can either determine the possible port graphs (including the edge orientations and edge numbers) or show that the given matrix is not realizable. Then, Theorem 8 can be used for testing the realizability. In [35], Biorci and Civalleri further established a more straightforward criterion without going through the actual realization procedure of the port graph topologically. It is shown that any admittance is realizable only if its sign matrix S_n satisfies a special form (called the *F matrix* in [35]). A rapid procedure that can reduce a sign matrix S_n to the form is also developed. Finally, the port graph can be directly determined and Theorem 8 can be used for testing the realizability of Y_n. It is noted that the method in [35] is not very efficient when Y_n contains too many zero entries, for there are 2^k possible sign matrices if k zero entries exist in Y_n. For this reason, [36] investigates a realization procedure that is particularly convenient when a large number of zero entries are present.

In addition to finding possible port graphs for the realization of Y_n, Boesch and Youla [37] focused on directly determining the inverse of the tree transformation matrix $\mathfrak{W}_{iL}$ of Theorem 8. It is shown in [37] that $\mathfrak{W}_{iL}^{-1}$ satisfies

$$\mathfrak{W}_{iL}^{-1} + \mathfrak{W}_{iL}^{-\mathrm{T}} = \frac{\operatorname{sgn} Y_n + U_n}{2} + I_n, \tag{5}$$

where the entries of sgn Y_n are ± 1 and $U_n \in \mathbb{R}^{n \times n}$ is the matrix whose entries are all 1. Through further showing that Y_n can always be converted into the canonical form that ensures $\mathfrak{W}_{iL}^{-1}$ to be triangular and by establishing a rapid determination of the form, $\mathfrak{W}_{iL}^{-1}$ can be easily calculated using (5). However, the restriction of this method is that Y_n must contain nonzero entries.

VI. REALIZABILITY OF ADMITTANCES WITH MORE THAN $n+1$ TERMINALS

As reviewed in the previous section, the realizability problem of the admittance as resistive n-port networks containing $n+1$ terminals has already been solved, although easy-to-check criteria can still be explored. This section reviews the development of more general cases, which are resistive n-port networks with more than $n+1$ terminals. A series of works were focused on this problem. However, unlike the $n+1$ case, this problem is still not completely solved as of today.

One of the most well-known methods is to expand the resistive n-port network containing $n+p$ terminals to the $(n+p-1)$-port one without changing the number of terminals, by properly adding $p-1$ new ports to form a new port graph $\widetilde{\mathcal{G}}_p$. It is required that $\widetilde{\mathcal{G}}_p$ be a tree of $\widetilde{\mathcal{G}}_p \cup \mathcal{G}_{ec}$, which converts the realization problem into the n'-port $(n'+1)$-terminal case that has already been solved. This methodology was originally discussed by Guillemin [38], without showing any realizability condition. Consequently, Swaminathan and Frisch [39] derived a necessary and sufficient condition for the admittance Y_n to be realizable as an n-port resistive network containing $n+2$ terminals, in terms of the entries of Y_n and a set of parameters. The relationship between the admittance $Y_k \in \mathbb{S}^k$ of the resistive k-port network N_k containing $k+p$ terminals and the admittance $Y_{k+1} \in \mathbb{S}^{k+1}$ of the $(k+1)$-port network N_{k+1} yielded by adding a new port to N_k is [39]:

$$Y_{k+1} = (Y_k \dotplus 0) + \sigma_k \sigma_k^{\mathrm{T}}, \tag{6}$$

where $\sigma_k = [p_1, p_2, \ldots, p_k, p_{k+1}]^{\mathrm{T}}$, and the kth row (column) of Y_{k+1} corresponds to the new port. Making use of (6) and Theorem 5, the following theorem is obtained.

Theorem 9: [39] A given matrix $Y_n \in \mathbb{S}^n$ can be realized by a resistive n-port network containing $n+2$ terminals, if and only if after a proper rearrangement of rows and columns, there exist $\mathfrak{W} = \mathfrak{W}_{1P_1} \dotplus \mathfrak{W}_{2P_2}$ and a set of parameters $p_1, p_2, \ldots, p_n, p$, such that the entries of $\mathfrak{W} Y_n \mathfrak{W}^{\mathrm{T}}$ satisfy

$$\begin{aligned} &(y_{a,b} - y_{a,b+1}) - (y_{a-1,b} - y_{a-1,b+1}) \\ &\qquad \geq (p_a - p_{a-1})(p_{b+1} - p_b) \geq 0, \\ &\text{for } a, b = 1, 2, \ldots, (m-2), \text{ and } b \geq a. \end{aligned}$$

$$\begin{aligned} &(y_{a,m-1} - y_{a-1,m-1}) \geq (p_a - p_{a-1})(p - p_{m-1}) \geq 0, \\ &\qquad \text{for } a = 1, 2, \ldots, (m-1), \end{aligned}$$

$$\begin{aligned} &(y_{i,j} - y_{i,j+1}) - (y_{i-1,j} - y_{i-1,j+1}) \\ &\qquad \geq (p_{i-1} - p_i)(p_j - p_{j+1}) \geq 0, \\ &\qquad \text{for } i, j = (m+1), (m+2), \ldots, n, \text{ and } j \geq i. \end{aligned}$$

$$\begin{aligned} &(y_{m,j} - y_{m,j+1}) \geq (p - p_m)(p_j - p_{j+1}) \geq 0, \\ &\qquad \text{for } j = m, (m+1), \ldots, n, \end{aligned}$$

$$\begin{aligned} &(p_a - p_{a-1})(p_j - p_{j+1}) \\ &\quad \geq -(y_{a,j} - y_{a,j+1}) + (y_{a-1,j} - y_{a-1,j+1}) \\ &\quad \text{for } a = 1, 2, \ldots, (m-1), \quad j = m, (m+1), \ldots, n, \end{aligned}$$

$$\begin{aligned} &(p_a - p_{a-1})(p - p_m) \geq (y_{a,m} - y_{a-1,m}) \\ &\qquad \text{for } a = 1, 2, \ldots, (m-1), \end{aligned}$$

$$(p - p_{m-1})(p - p_m) \geq -y_{m-1,m},$$

$$\begin{aligned} &(p - p_{m-1})(p_j - p_{j+1}) \geq (y_{m-1,j} - y_{m-1,j+1}) \\ &\qquad \text{for } j = m, (m+1), \ldots, n, \end{aligned}$$

where subscripts m and n are utilized to index the rows or columns in positions $m-1$ or less, and i and j are used for the rows or columns above $m-1$.

Through eliminating parameters $p_1, p_2, \ldots, p_n, p$, [39] further derives a necessary condition for realizability based on Theorem 9. Moreover, [39] generalizes the necessary condition to the general $n+p$ case with $p > 2$ ($\mathcal{G}_p$ consists of multiple subtrees) by shorting-circuiting all the ports except those corresponding to any two subtrees. However, no necessary and sufficient condition is available.

Before reviewing further investigations on the realization with more than $n+1$ terminals, the works on the parallel connection of two resistive n-port networks are first introduced. If there is a one-to-one correspondence between the ports and the terminals of two n-port networks N_1 and N_2 to make the corresponding ports be incident at corresponding terminals, then N_1 and N_2 are called *compatible* [40]. Unlike the $(n+1)$-terminal case (implied from (3)), the admittance Y_n of the network N containing $(n+p)$ terminals that are parallel between N_1 and N_2 cannot always satisfy $Y_n = Y_n^{(1)} + Y_n^{(2)}$, where $Y_n^{(1)}$ and $Y_n^{(2)}$ are admittances of N_1 and N_2. Therefore, [40] and [41] investigate conditions for $Y_n = Y_n^{(1)} + Y_n^{(2)}$. It is derived in [42], [43] that $Y_n = W_e G W_e^{\mathrm{T}}$, where $W_e = W_1 - W_1 G W_2^{\mathrm{T}} (W_2 G W_2^{\mathrm{T}})^{-1} W_2$. Furthermore, W_e also satisfies $\hat{U} = W_e^T \hat{V}$ and $\hat{I} = W_e \hat{J}$. Since W_e plays a similar role as the fundamental cut-set matrix for the $(n+1)$-terminal case, W_e is called the *modified cut-set matrix*. A necessary and sufficient condition for $Y_n = Y_n^{(1)} + Y_n^{(2)}$ is presented in [40] as follows.

Theorem 10: [40] The parallel connection of two compatible resistive n-port networks N_1 and N_2 yields $Y_n = Y_n^{(1)} + Y_n^{(2)}$, if and only if their modified cut-set matrices with identical row and column ordering are equal.

Remark 3: Theorem 10 also applies to networks with negative elements, provided that their modified cut-set matrices exist.

Reference [44] further discusses the realization method of resistive n-port networks containing $n+2$ terminals, which is still based on the expansion method applied in [38], [39]. The network is decomposed into three networks in parallel, one of which contains both positive and negative elements. It is shown that if a matrix is realizable by such a class of networks, then the realization method can be applied. But the sufficiency cannot be guaranteed. Furthermore, [45] generalizes the discussion to the $(n+p)$-terminal case with $p > 2$. In [46], a method regarding the conductances of $n+1$ elements incident to common terminals as $n+1$ parameters is proposed to realize the resistive n-port network containing $n+1$ terminals. The advantage is that the number of elements in the realization can be well controlled. Reference [47] defines the *network of departure* N_d and the *padding n-port network* N_p, and shows that any resistive n-port network can be regarded as a parallel connection of such two networks. It also points out that many previous works including [38], [39], [44] can be stated in terms of such two networks, where the main difference is the approach of obtaining the padding network N_p. Furthermore, a necessary and sufficient condition for the realizability of the modified cut-set matrix is derived. Then, a new realization approach of a given admittance as the resistive n-port network with $n+2$ terminals is developed. The procedure is based on the realization of the modified cut-set matrix as the required padding network N_p, where the construction of the modified cut-set matrix needs a trial-and-error approach. As a consequence, [48] derives two sufficient conditions for Y_n to be realizable by the resistive n-port network containing $n+2$ terminals, one of which is only in terms of the entries of Y_n. After the 1970s, there was not much effort in investigating the synthesis of resistive n-port networks due to the interest declining, and the realizability problem of the $(n+p)$-terminal case with $p \geq 2$ remains not completely solved even for the case of $p = 2$ [54].

VII. RECENT RESULTS

Chen *et al.* [12] recently derived some new results on the realization problem of resistive n-port networks containing $2n$ terminals. In addition to other classes of resistive n-port networks containing more than $n+1$ terminals, such a class of networks is an essential case. Using the complete graph to denote its network graph, the symmetric topological property of an n-port network containing $2n$ terminals shows that the realizability condition should be independent of the structures and orientations of the ports, which may be simpler than other cases. Although it may be impossible for any resistive n-port network to be always equivalent to the one with $2n$ terminals, it is only needed to focus on investigating those that do not contain the equivalence. Therefore, the investigation on its realizability is theoretically important.

It is shown in [15] that a sufficient condition for any $Y_n \in \mathbb{S}^n$ to be realizable by the resistive n-port network containing $2n$ terminals is that Y_n is a dominant matrix. Although [38], [39] have discussed networks containing more than $n+2$ terminals, including the $2n$-terminal case, a necessary and sufficient condition for the realizability is not available. In [12], Chen *et al.* derived a necessary and sufficient condition for realizability based on the existence of a parameter matrix, as follows.

Theorem 11: [12] A matrix $Y_n \in \mathbb{S}^n$ can be realized as the admittance of an n-port resistive network N with $2n$ terminals, if and only if there exists a matrix $P \in \mathbb{R}^{(2n-1)\times(n-1)}$ in the form of

$$P = \left[\begin{array}{cccc} \gamma_1 & \gamma_2 & \cdots & \gamma_{n-1} \end{array}\right]$$

with

$$\gamma_k := \left[p_1^{(k)}\ p_{n+1}^{(k)}\ \cdots\ p_k^{(k)}\ p_{n+k}^{(k)}\ p_{k+1}^{(k)}\ 0\ \cdots p_{n-1}^{(k)}\ 0\ p_n^{(k)}\right]^{\mathrm{T}}$$

for $1 \le k \le n-1$, such that

$$\begin{aligned}\max\{(\alpha_i - \beta_{i-1})^{\mathrm{T}}(\beta_j - \alpha_j),\ (\alpha_i - \beta_i)^{\mathrm{T}}(\beta_{j-1} - \alpha_j)\} \le y_{ij} \\ \le \min\{(\alpha_i - \beta_{i-1})^{\mathrm{T}}(\beta_{j-1} - \alpha_j),\ (\alpha_i - \beta_i)^{\mathrm{T}}(\beta_j - \alpha_j)\}\end{aligned}$$

for $1 \le i < j \le n$ and

$$y_{ii} \ge -(\alpha_i - \beta_{i-1})^{\mathrm{T}}(\alpha_i - \beta_i), \qquad 1 \le i = j \le n,$$

where α_l^{T} is the $(2l-1)$th row of P with $1 \le l \le n$, β_m^{T} is the $2m$th row of P with $1 \le m \le n-1$, and $\beta_0 = \beta_n := 0_{(n-1)\times 1}$.

It is noted that Theorem 11 can be seen as a generalization of the work by Swaminathan and Frisch for the $(n+2)$-terminal case (Theorem 9), but its condition is much simpler than that of Theorem 9, for there is no need to find proper rearrangement of rows and columns for Y_n and it is not necessary to check the existence of $\mathfrak{W}$, which needs certain additional procedures. Moreover, it is clear that the condition of Theorem 11 is more uniform than that of Theorem 9, and there is one and only one entry of Y_n in each inequality in Theorem 11. The formulas for the values of the elements are also derived in [12], as follows.

Theorem 12: [12] If a matrix $Y_n \in \mathbb{S}^n$ can be realized as the admittance of an n-port resistive network with $2n$ terminals whose graph is as shown in Fig. 5, where the orientations of the ports are from vertices A_{2k-1} to A_{2k} with $1 \le k \le n$, then the conductances of the resistors of the edges are given by

$$g_{2r-1,2s} = y_{r,s} + (\alpha_r - \beta_{r-1})^{\mathrm{T}}(\alpha_s - \beta_s),$$

for $1 \le r \le s \le n$, and

$$\begin{aligned} g_{2r-1,2s-1} &= -y_{r,s} - (\alpha_r - \beta_{r-1})^{\mathrm{T}}(\alpha_s - \beta_{s-1}), \\ g_{2r,2s-1} &= y_{r,s} + (\alpha_r - \beta_r)^{\mathrm{T}}(\alpha_s - \beta_{s-1}), \\ g_{2r,2s} &= -y_{r,s} - (\alpha_r - \beta_r)^{\mathrm{T}}(\alpha_s - \beta_s), \end{aligned}$$

for $1 \le r < s \le n$, where α_k and β_k are obtained from the parameter matrix P as defined in Theorem 11, and $g_{h,l}$ denotes the conductance of the element connecting vertices A_h and A_l for $1 \le h < l \le 2n$.

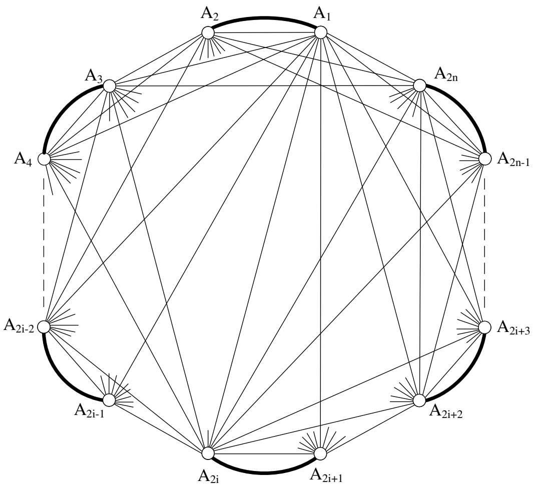


Fig. 5. The complete graph of an n-port resistive network with $2n$ terminals, where the bold line segments correspond to the edges of the port graph (see [12]).

Define $N_{i,j} := \max\{(\alpha_i - \beta_{i-1})^{\mathrm{T}}(\beta_j - \alpha_j),\ (\alpha_i - \beta_i)^{\mathrm{T}}(\beta_{j-1} - \alpha_j)\}$, and $M_{i,j} := \min\{(\alpha_i - \beta_{i-1})^{\mathrm{T}}(\beta_{j-1} - \alpha_j),\ (\alpha_i - \beta_i)^{\mathrm{T}}(\beta_j - \alpha_j)\}$ for $1 \le i < j \le n$. Further define $L_i := (\alpha_i - \beta_{i-1})^{\mathrm{T}}(\beta_i - \alpha_i)$ for $1 \le i \le n$. Together with the property of paramountcy, a constraint on entries of the parameter matrix P is also derived in [12], as follows.

Corollary 1: [12] If the condition of Theorem 11 holds, then the matrix P must satisfy $M_{i,j} \ge N_{i,j}$ and $L_i \ge \max\{\ |M_{i,j}|,\ |N_{i,j}|\ \}$, where $1 \le i < j \le n$.

To summarize, [12] derives a necessary and sufficient condition for any real symmetric matrix to be realizable by the resistive n-port network containing $2n$ terminals, and establishes the formulas for the values of the elements. Since Theorem 11 is based on the existence of a parameter matrix, the condition may be tested by the trial-and-error approach based on computer programming. To enhance the practical meaning of the result, improved algorithms of constructing the parameter matrix will be considered in the future.

VIII. CONCLUSION

This survey has briefly reviewed the realization problem of resistive n-port networks. A series of results from the 1950s to the 1970s have been discussed, including the realization problem for the case of $n \le 3$, properties of general resistive n-port networks, and the realizability of admittances as resistive n-port networks containing $n+1$ and more than $n+1$ terminals, respectively. In addition, some recent results on the realization problem of resistive n-port networks containing $2n$ terminals have been presented. This survey is intended to provide some solid ground for further research and development in this domain, which leaves many important and interesting issues to be further explored.

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